Fig. 1

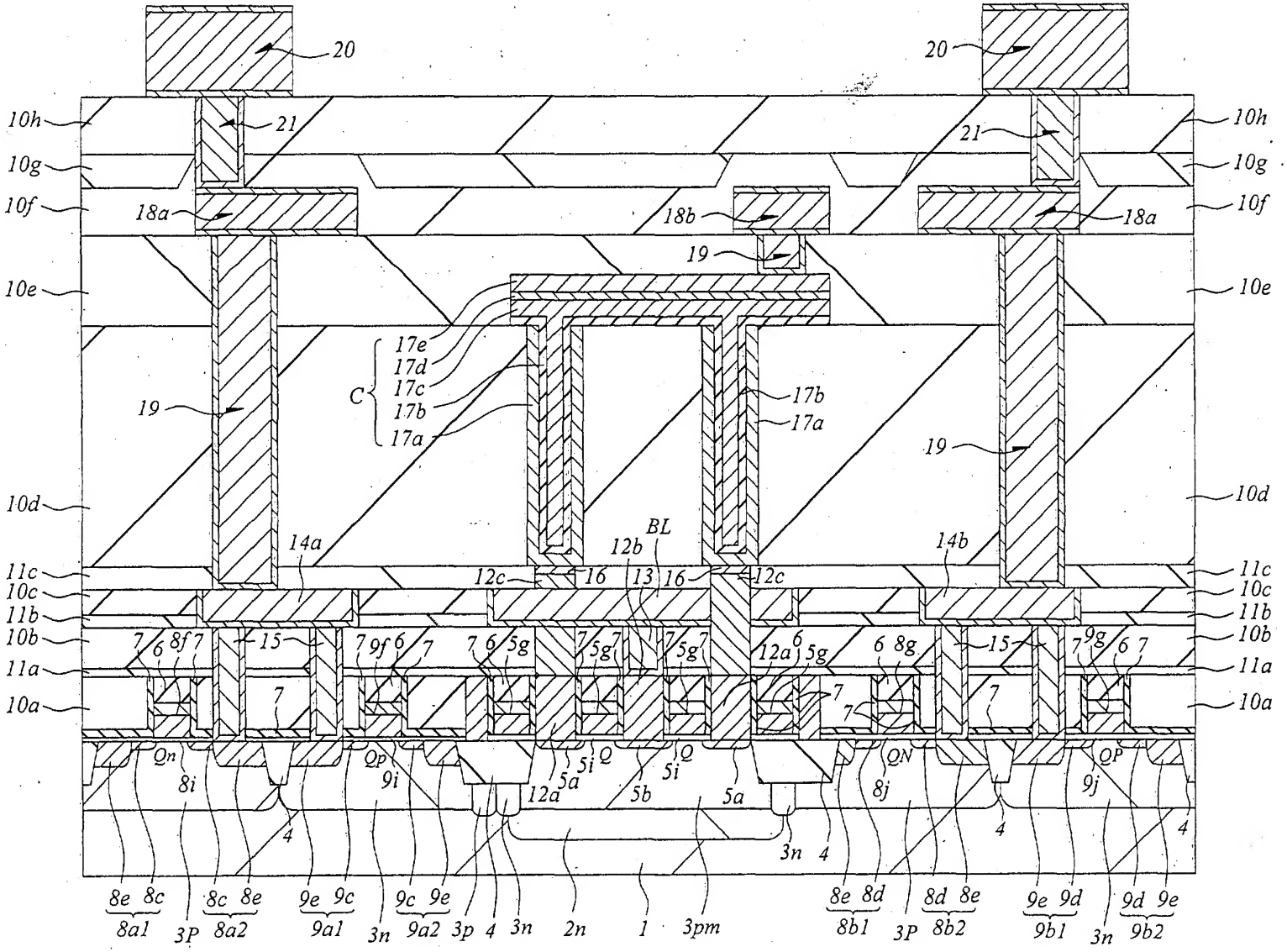
20
21
10h
10g
10f
18a
18b
19
10e
17e
17d
17c
17b
17a
C
10d
14a
14b
BL
12b
12c
16
13
11c
10c
11b
10b
11a
10a
15
12a
5g
9g
8g
8f
9f
Qn
Qp
QN
QP
8i
9i
8j
9j
5a
5b
5i
Q
4
3n
3p
3P
2n
1
3pm
8e 8c
8a1
8c 8e
8a2
9e 9c
9a1
9c 9e
9a2
8e 8d
8b1
8d 8e
8b2
9e 9d
9b1
9d 9e
9b2
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA

Fig. 2

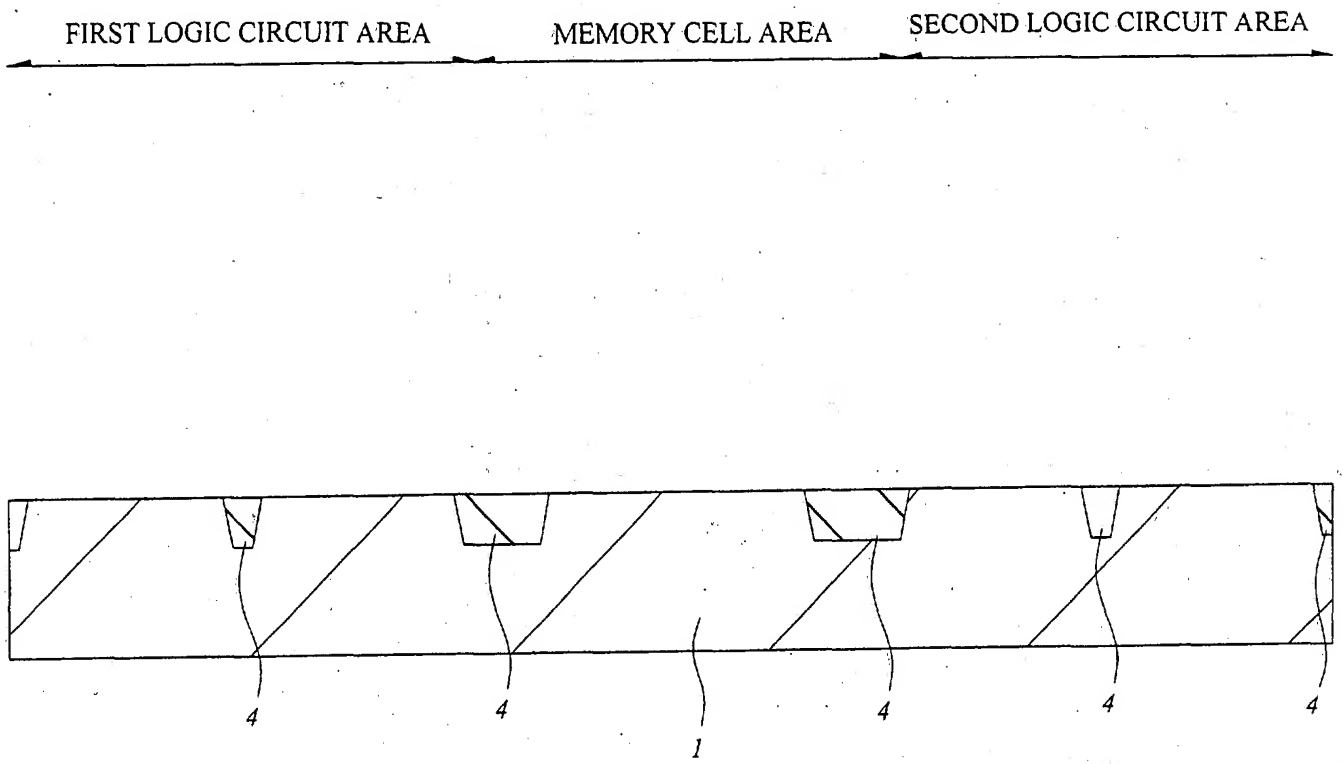
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
4
4
1
4
4
4

Fig. 3

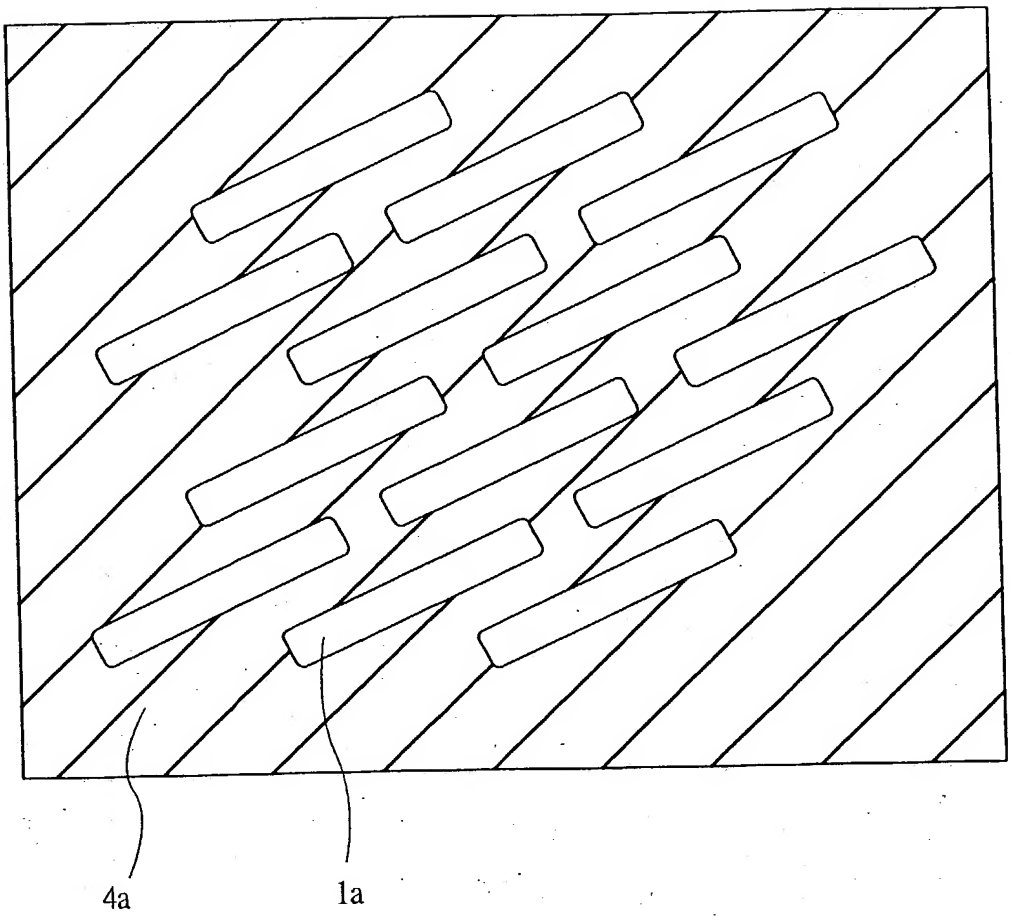

Fig. 4

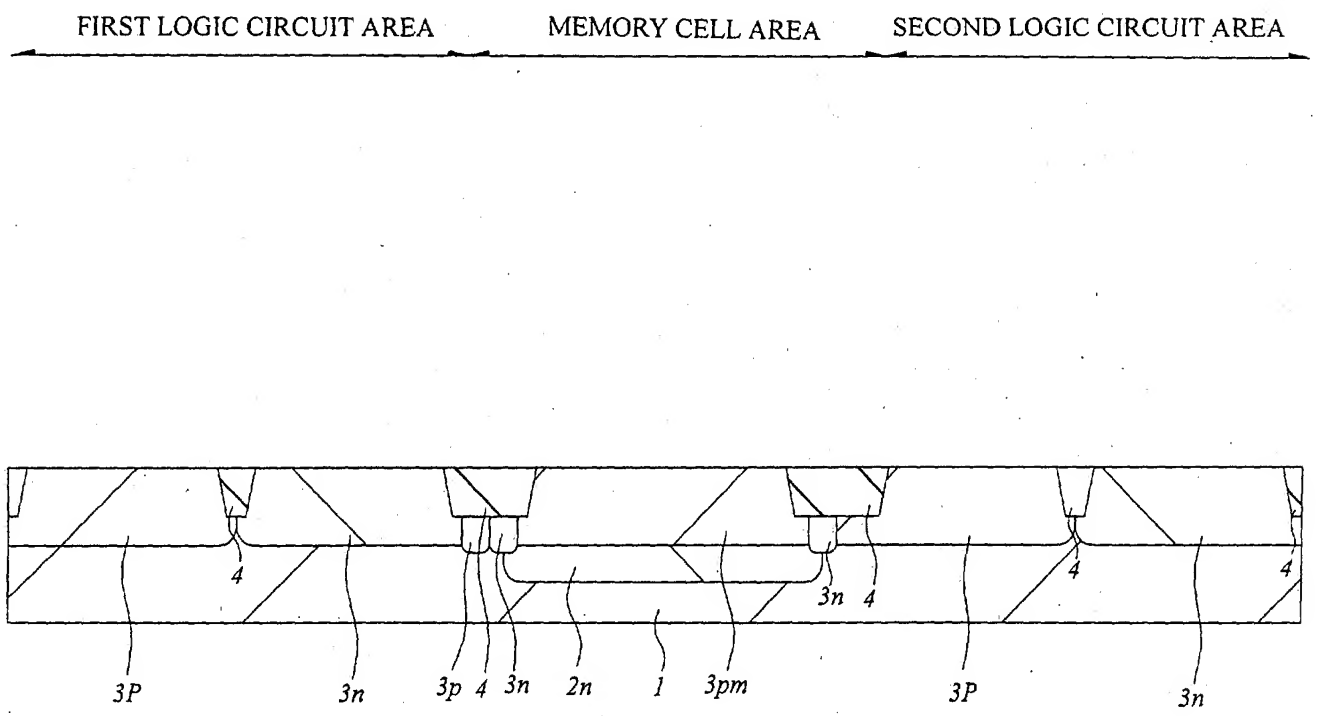
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 5

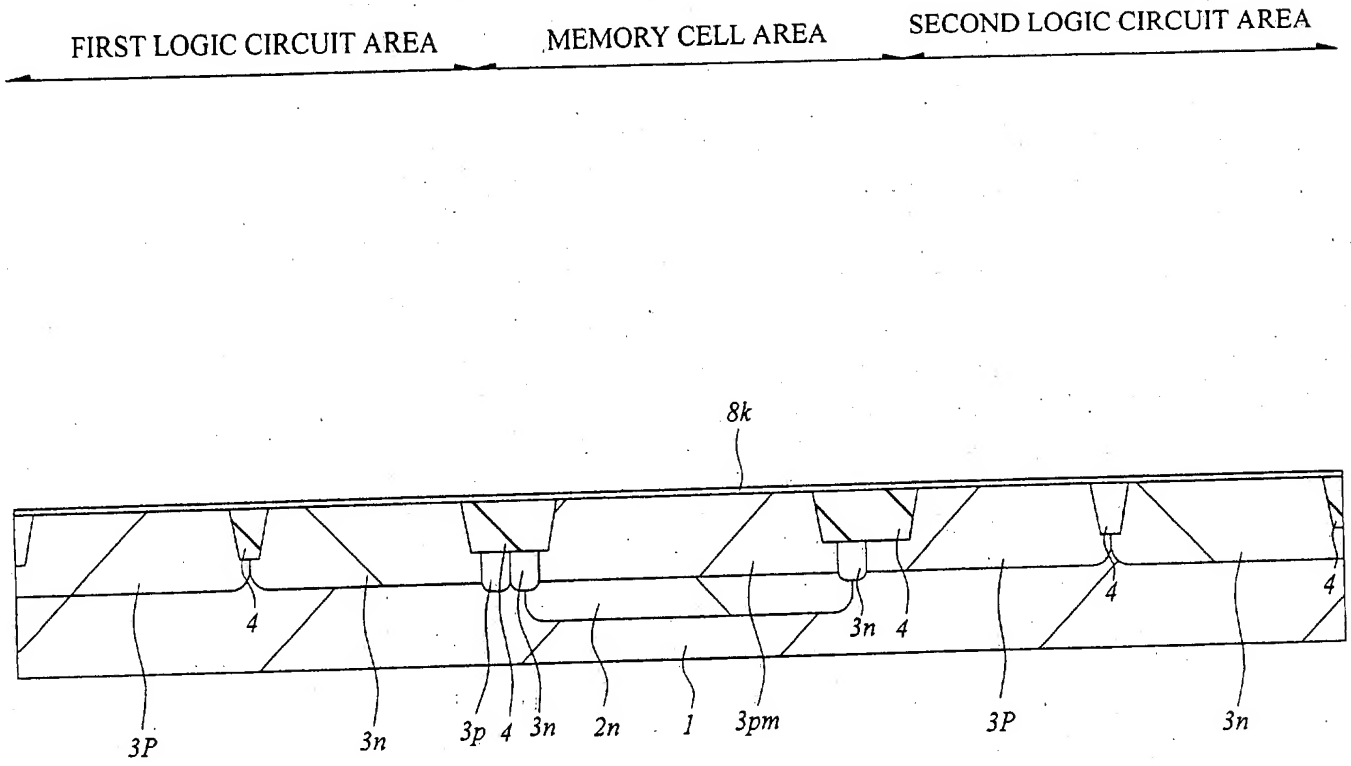
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8k
4
3P
3n
3p
4
3n
2n
1
3pm
3n
4
3P
4
3n
4

Fig. 6

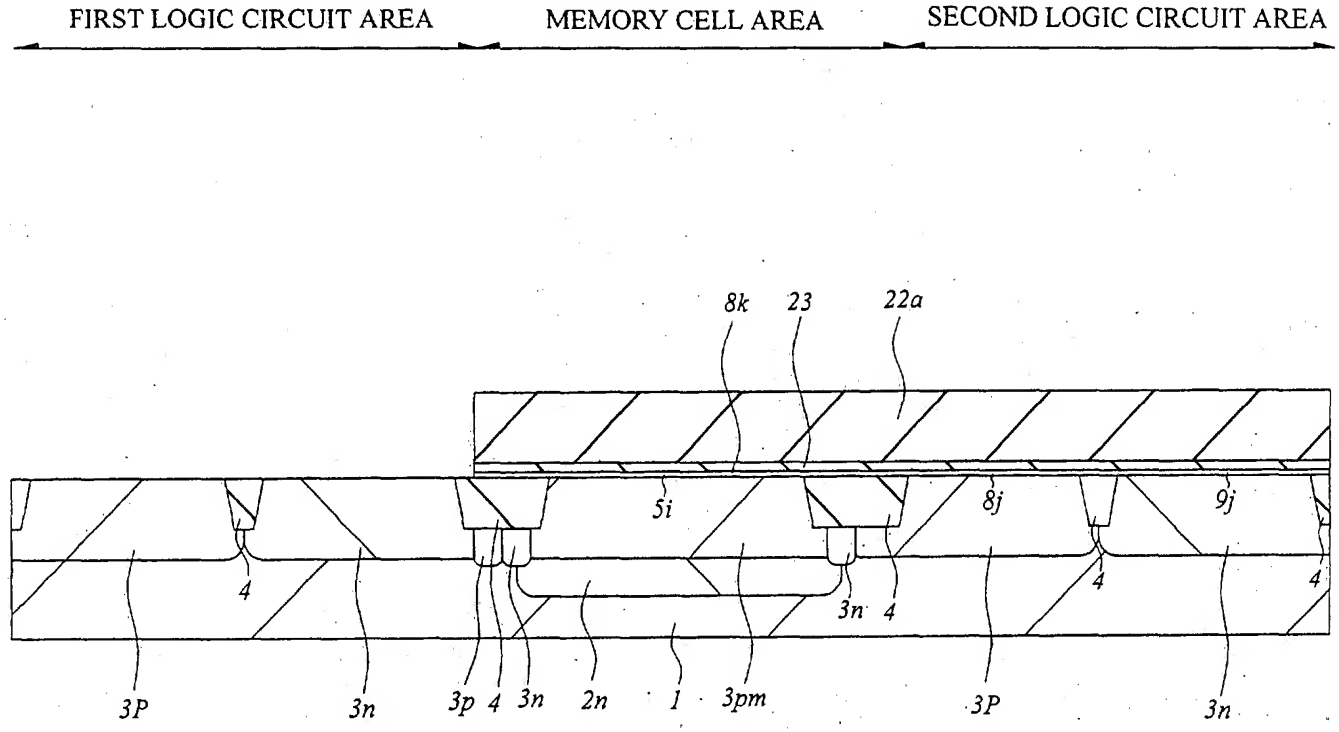
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8k
23
22a
5i
8j
9j
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 7

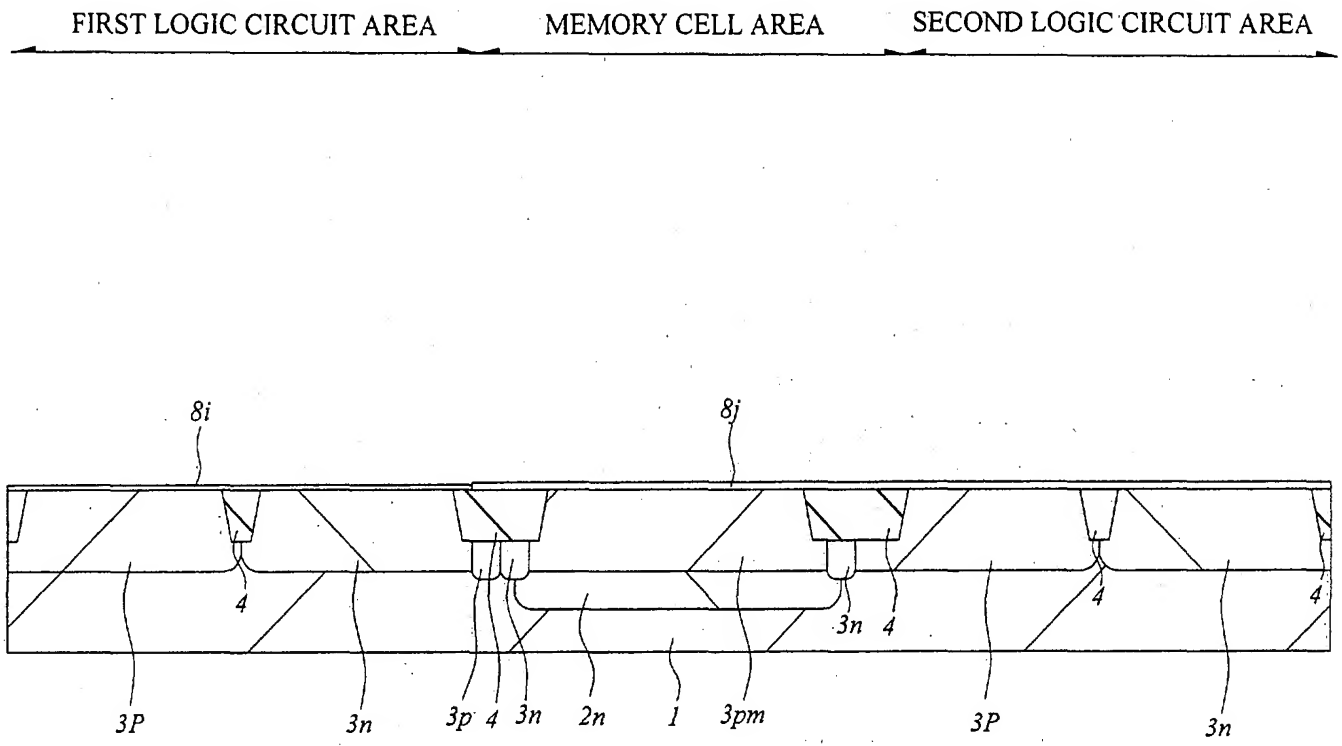
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8i
8j
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 8

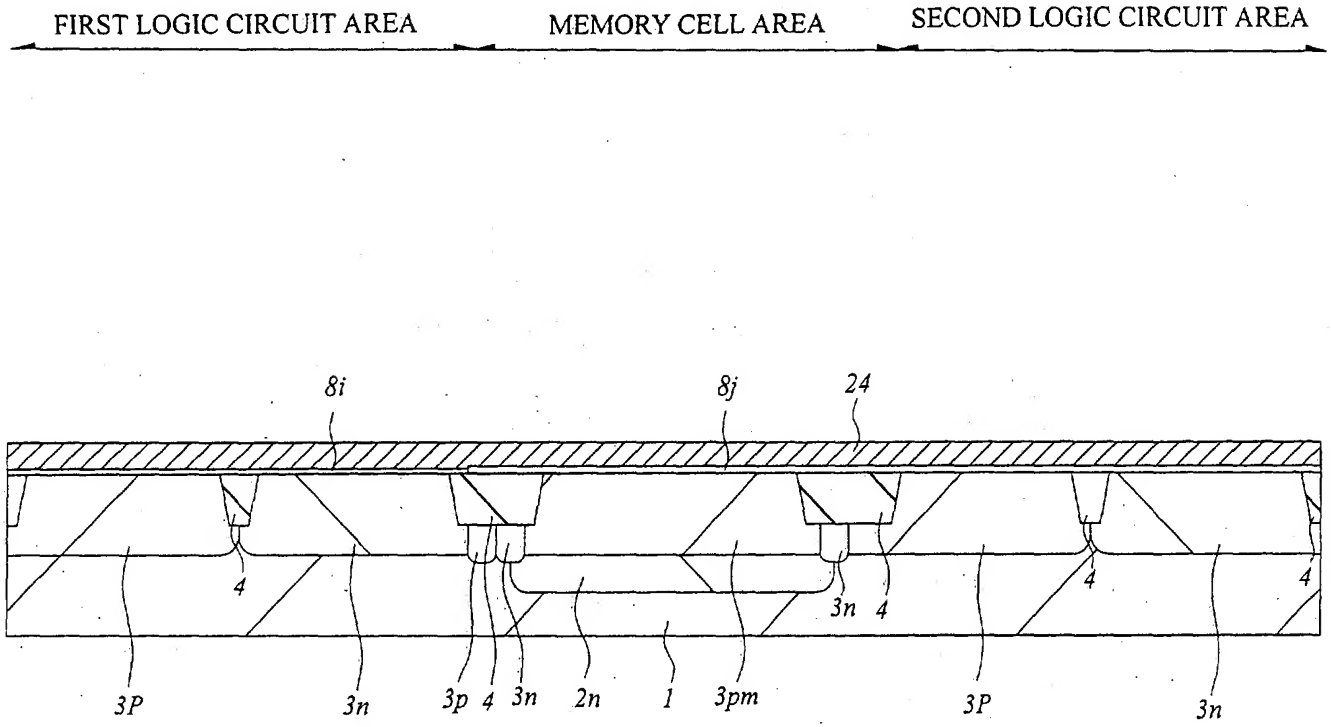
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8i
8j
24
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 9

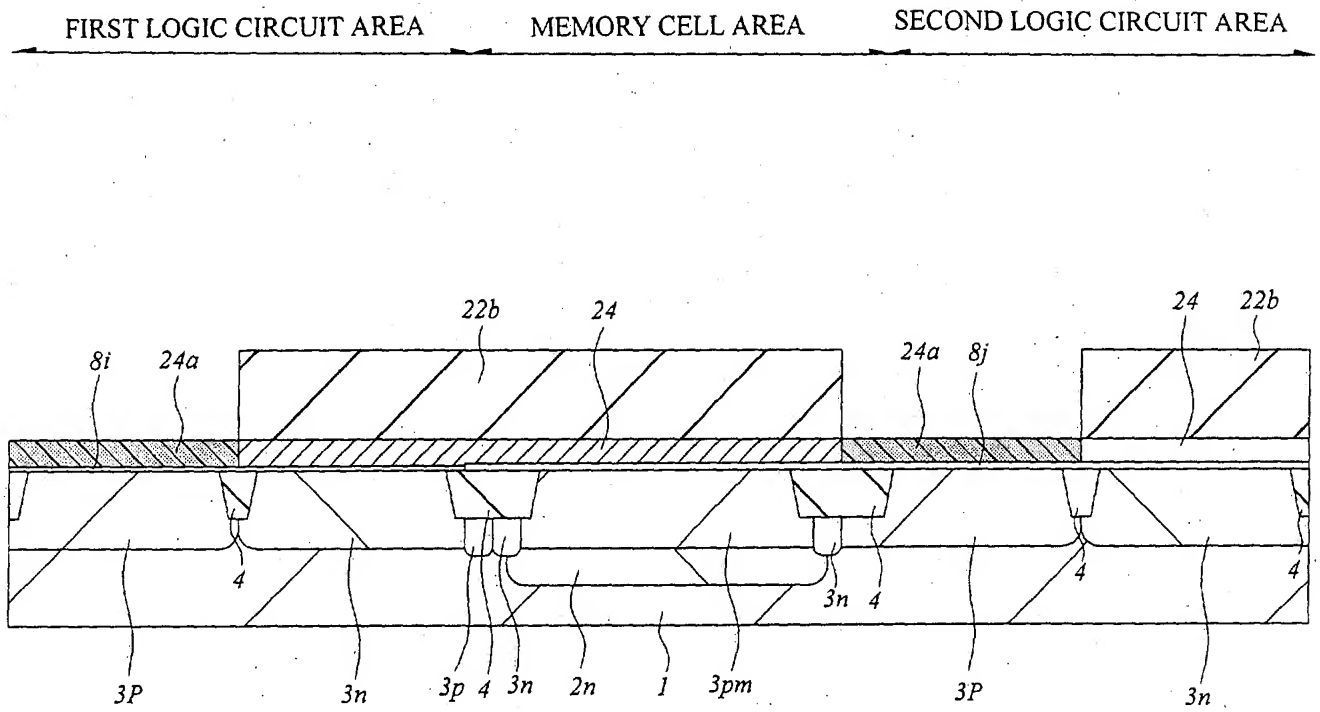
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22b
24
24
22b
8i
24a
24a
8j
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 10

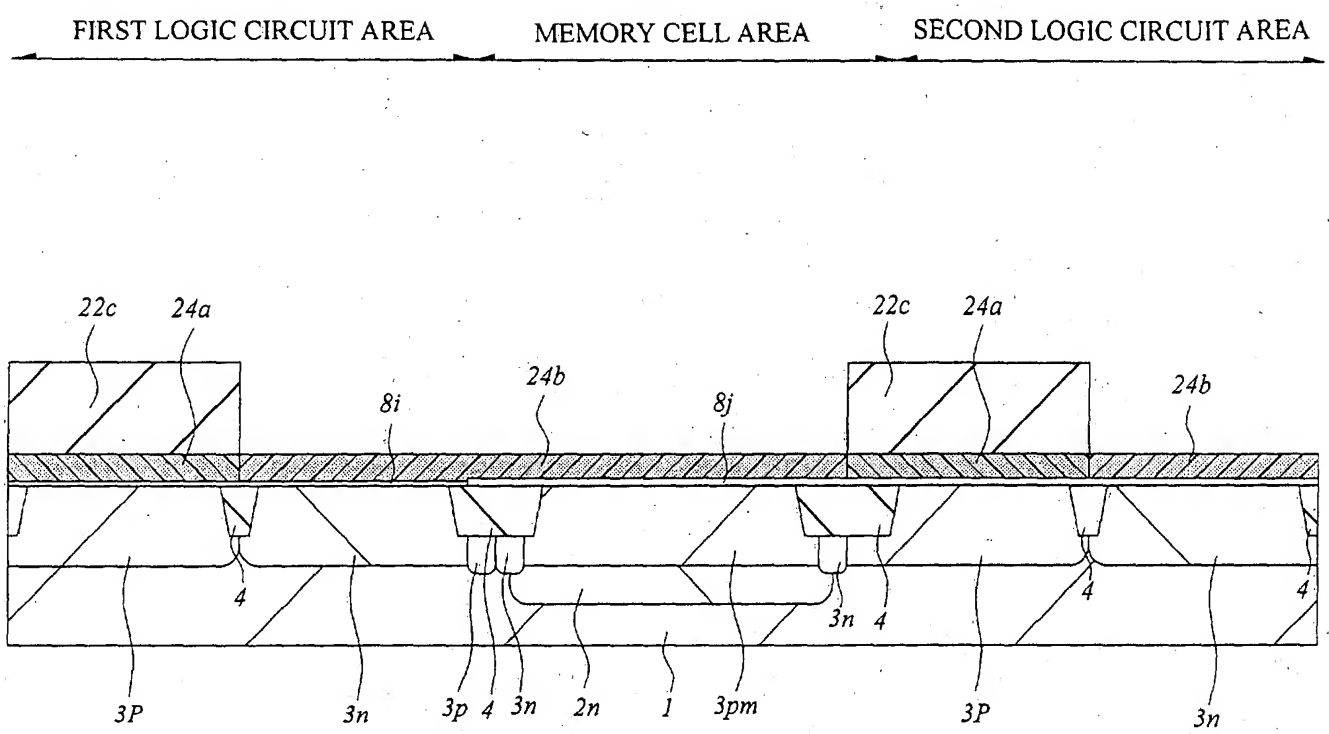
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22c
24a
8i
24b
8j
22c
24a
24b
4
3n
4
4
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 11

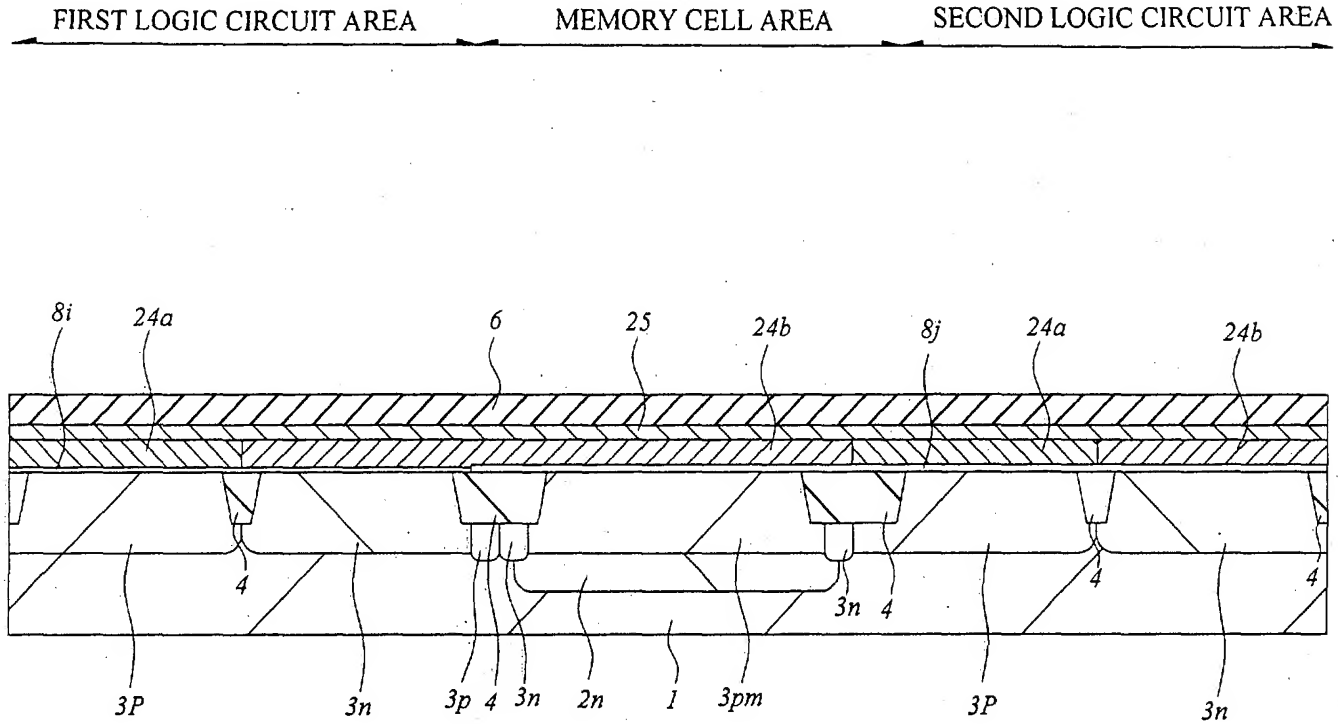
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8i
24a
6
25
24b
8j
24a
24b
4
4
4
4
3n
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 12

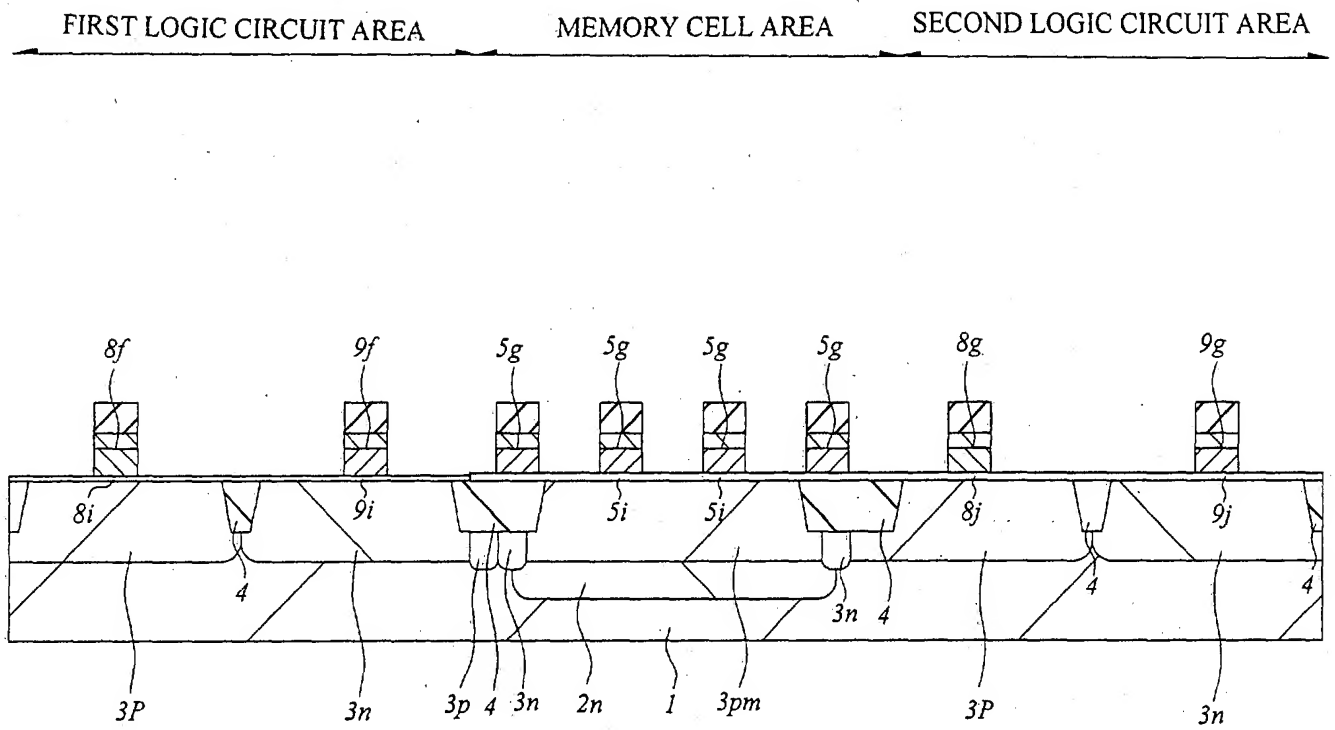
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g
5g
5g
5g
8g
9g
8i
9i
5i
5i
8j
9j
4
4
3n
4
4
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 13

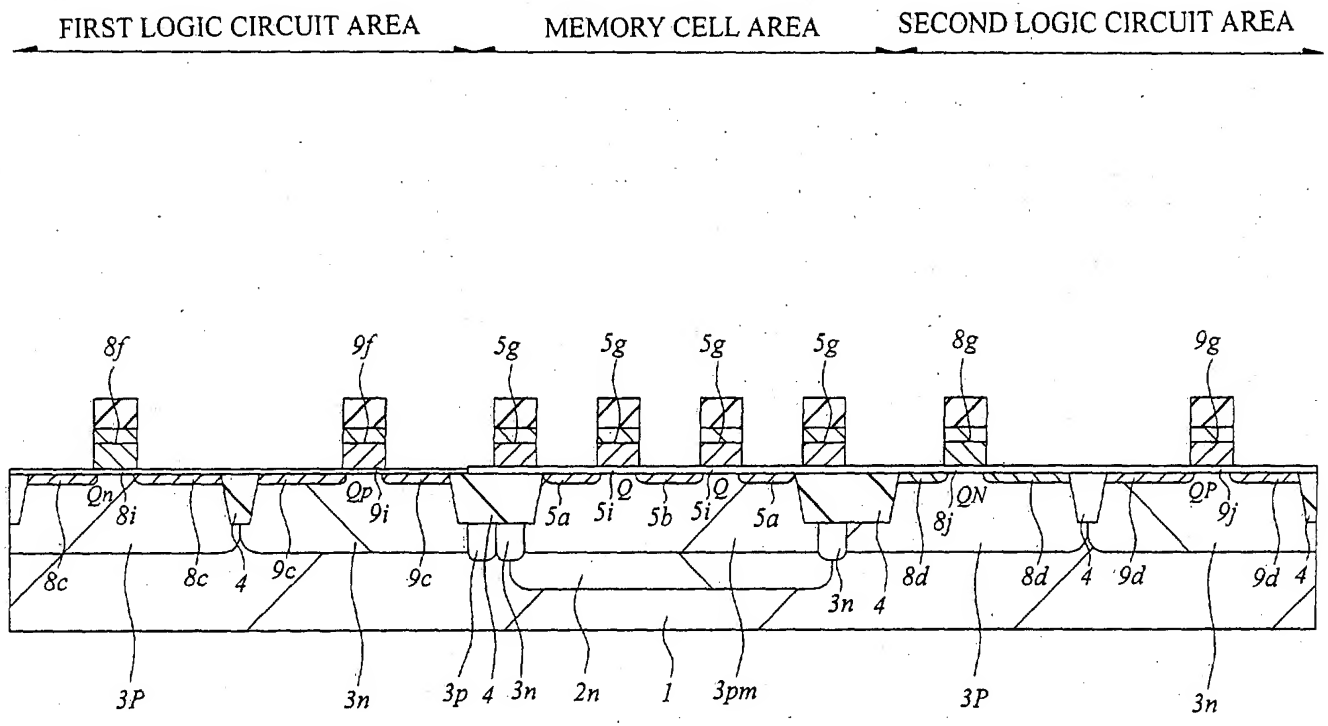
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g
5g
5g
5g
8g
9g
Qn
8i
Qp
9i
5a
5i
Q
5b
5i
Q
5a
8j
QN
QP
9j
8c
8c
4
9c
9c
3n
4
8d
8d
4
9d
9d
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 14

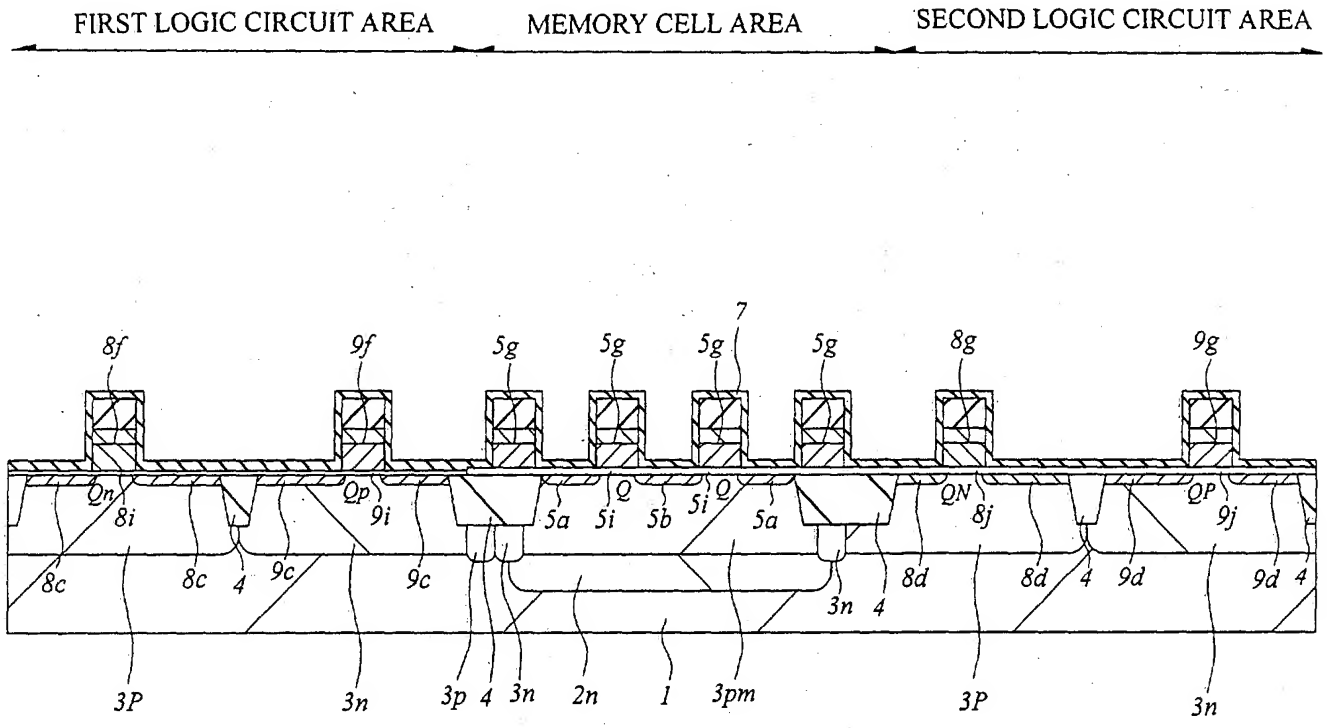
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g
5g
5g
7
5g
8g
9g
Qn
8i
Qp
9i
5a
5i
Q
5b
5i
Q
5a
QN
8j
QP
9j
8c
8c
4
9c
9c
3n
4
8d
8d
4
9d
9d
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 15

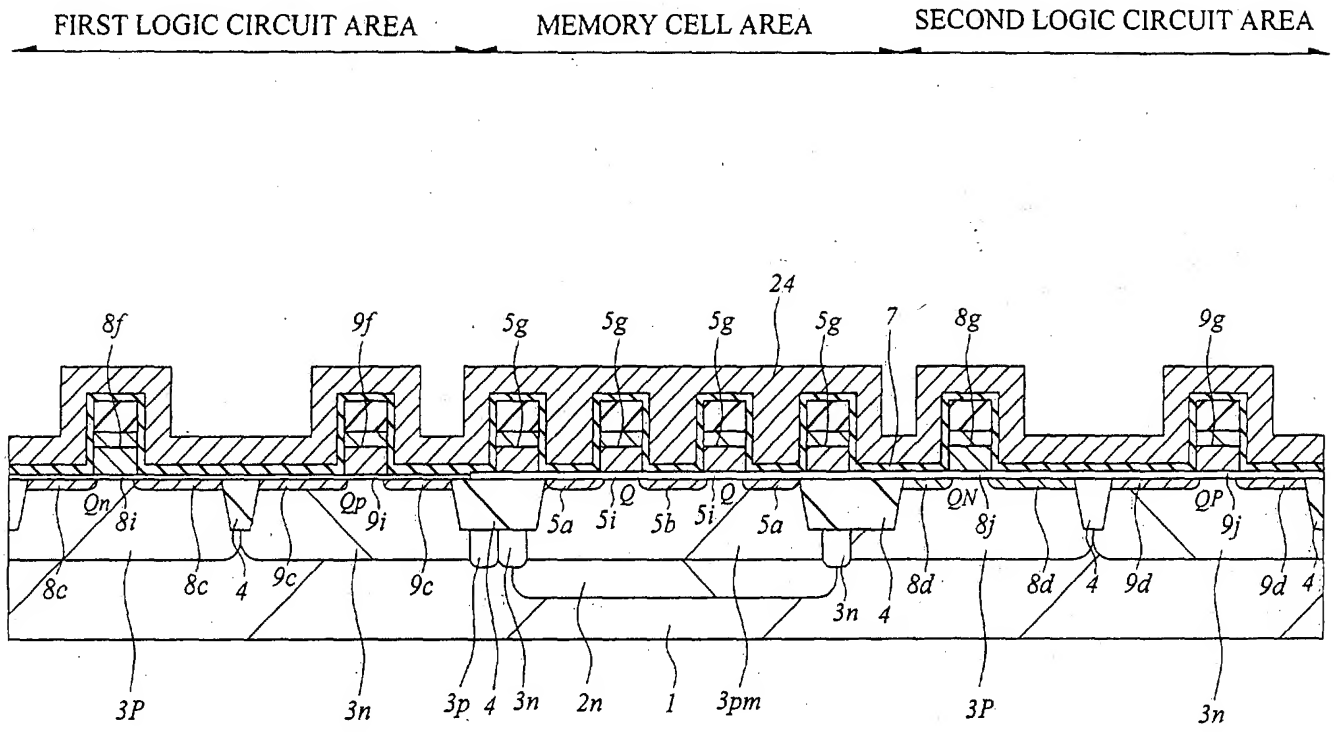
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
24
8f
9f
5g
5g
5g
5g
7
8g
9g
Qn
8i
Qp
9i
Q
Q
QN
QP
5a
5i
5b
5i
5a
8j
9j
8c
8c
4
9c
9c
3n
4
8d
8d
4
9d
9d
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 16

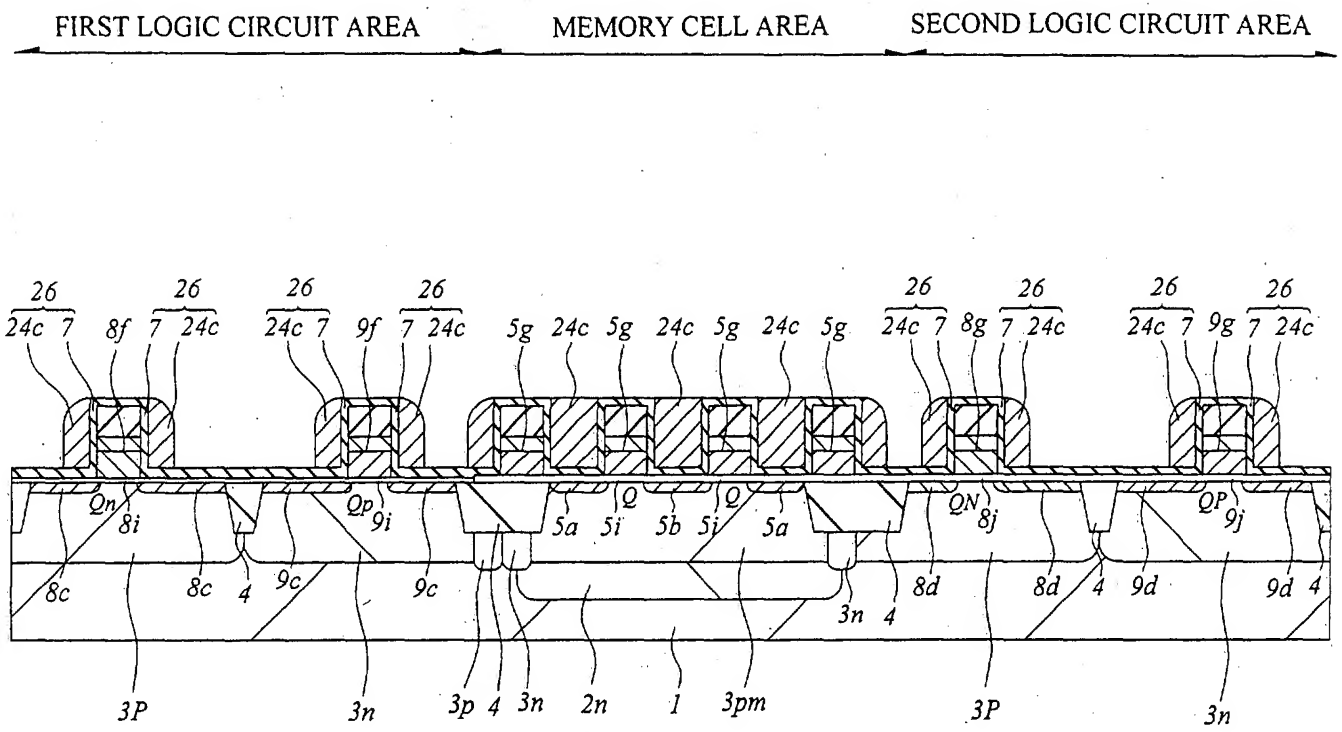
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
26
24c 7 8f 7 24c
26
24c 7 9f 7 24c
26
5g 24c 5g 24c 5g 24c 5g
26
24c 7 8g 7 24c
26
24c 7 9g 7 24c
Qn
8i
Qp
9i
Q
5a 5i 5b 5i 5a
QN
8j
QP
9j
8c
8c 4 9c
9c
3n 4
8d
8d 4 9d
9d 4
3P
3n
3p 4 3n
2n
1
3pm
3P
3n

Fig. 17

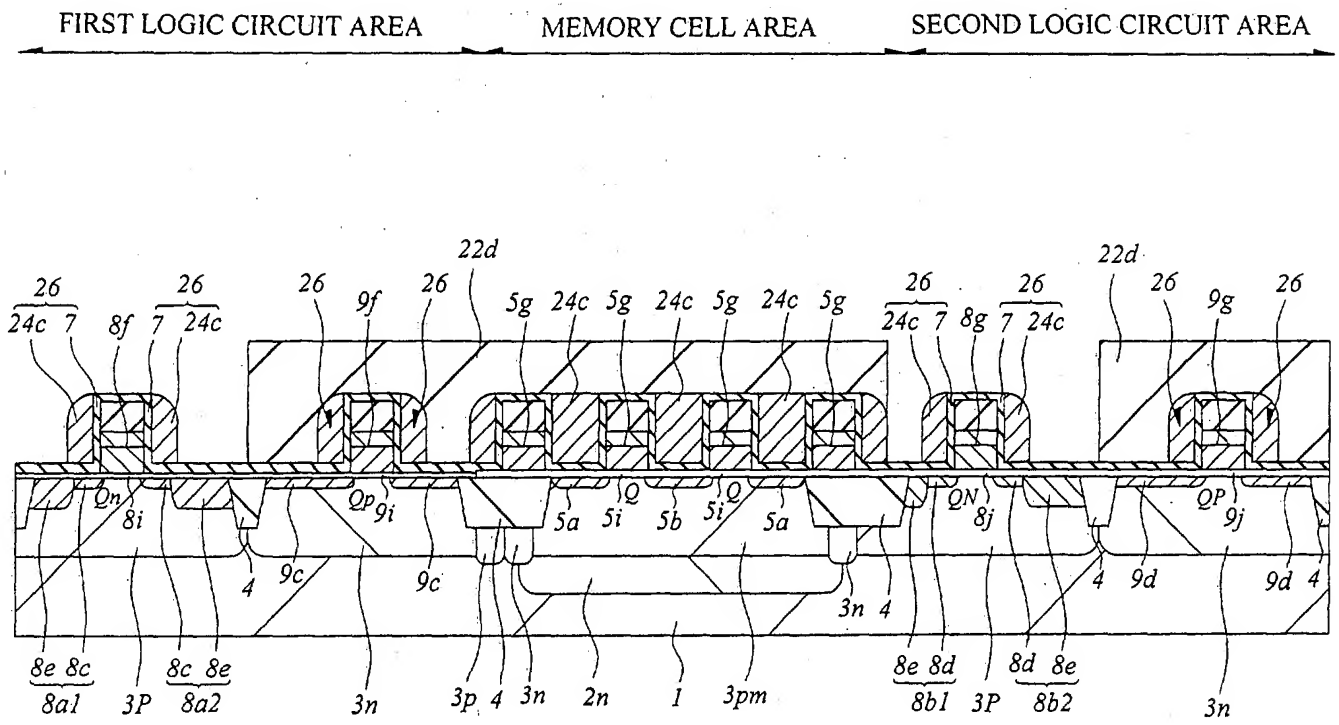
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
26
24c 7
8f
7 24c
9f
22d
5g 24c 5g 24c 5g 24c 5g
8g
9g
Qn
8i
Qp
9i
5a 5i 5b 5i 5a
QN
8j
QP
9j
4
9c
9d
3n 4
8e 8c
8a1
3P
8c 8e
8a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
8d 8e
8b2

Fig. 18

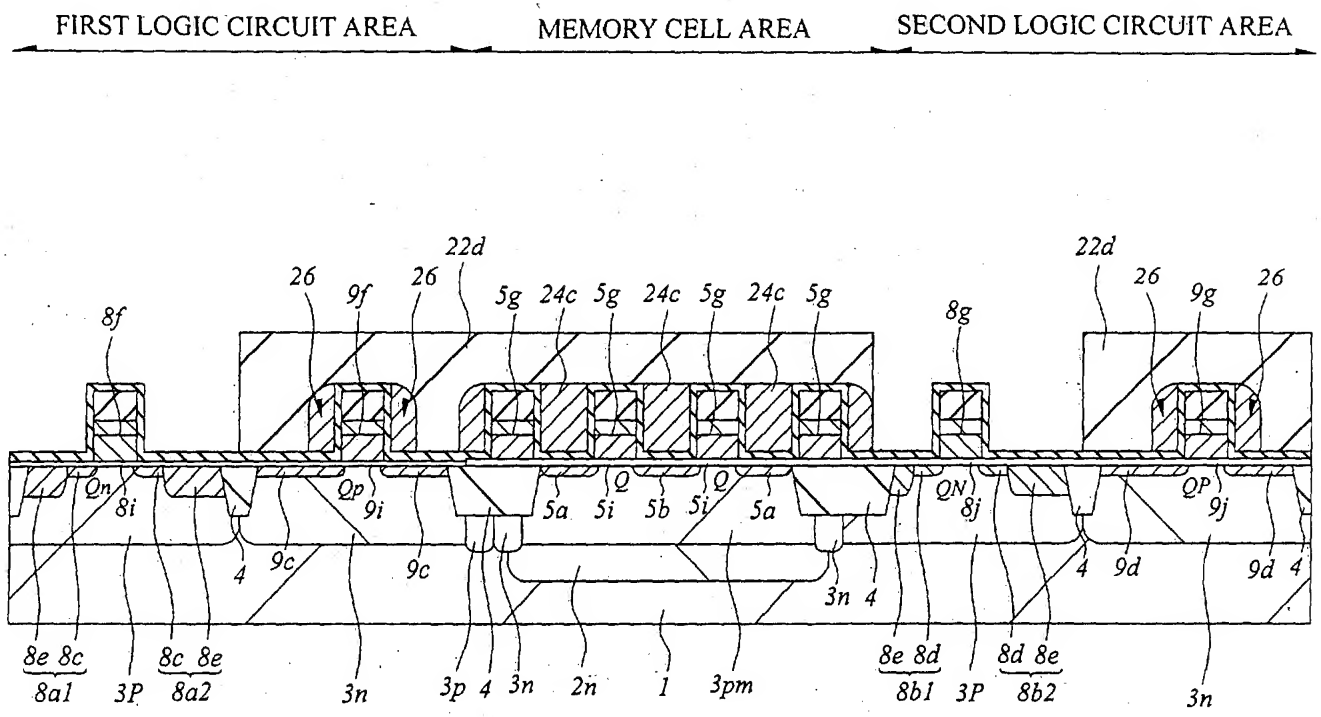
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22d
26
9f
26
22d
5g
24c
5g
24c
5g
24c
5g
8f
8g
26
9g
26
Qn
8i
Qp
9i
Q
Q
QN
8j
QP
9j
5a
5i
5b
5i
5a
4
9c
9c
3n
4
4
9d
9d
4
8e 8c
8a1
3P
8c 8e
8a2
3n
3p
4
3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
3n

Fig. 19

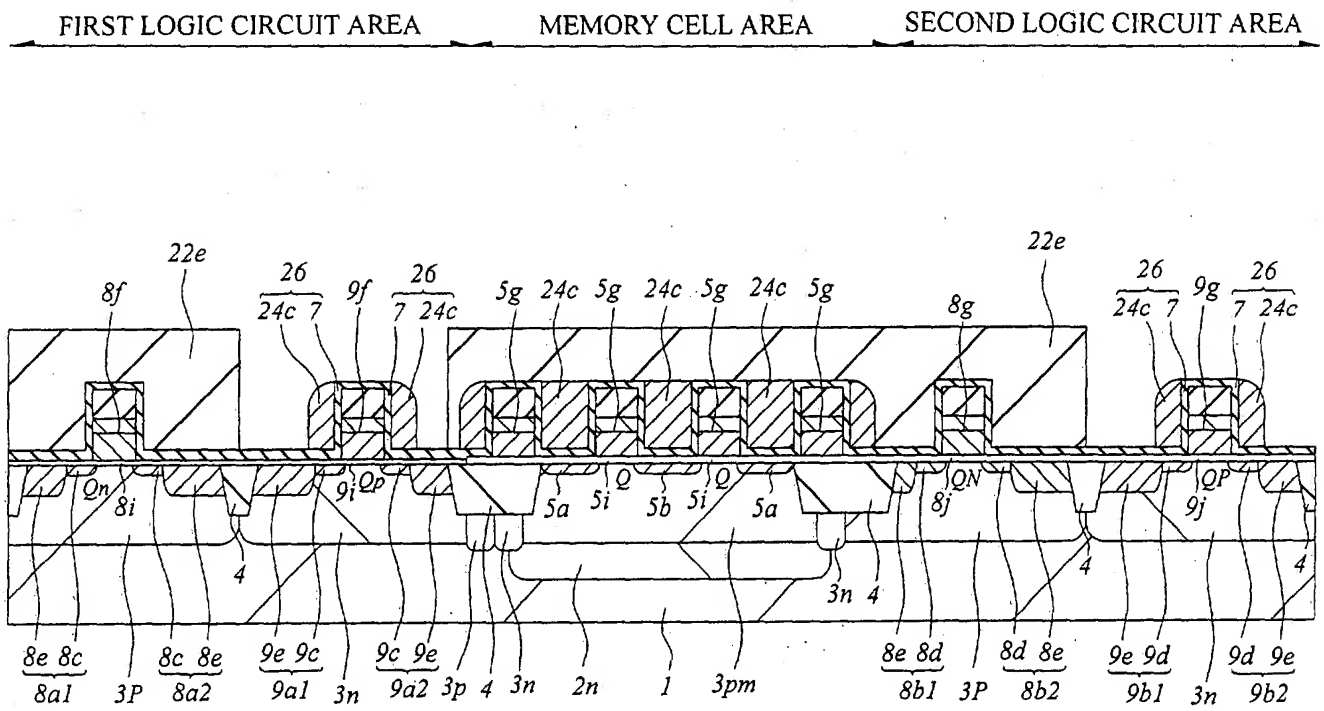
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22e
8f
26
24c 7
9f
26
7 24c
5g 24c 5g 24c 5g 24c 5g
8g
22e
26
24c 7
9g
26
7 24c
Qn
8i
9i
QP
5a 5i Q 5b 5i Q 5a
8j
QN
9j
QP
4
3n 4
4
4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p
4
3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 20

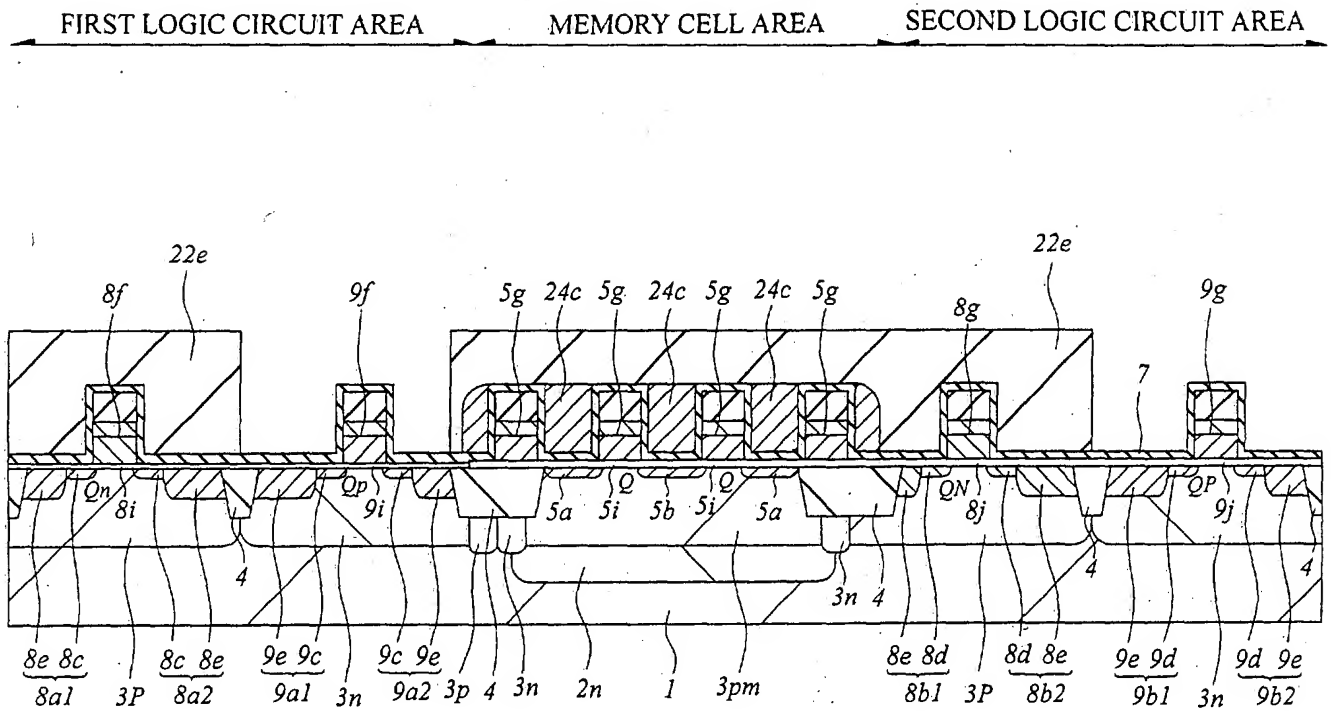
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22e
8f
9f
5g 24c 5g 24c 5g 24c 5g
8g
22e
9g
7
Qn
8i
Qp
9i
5a 5i 5b 5i 5a
Q
Q
QN
8j
QP
9j
4
4
4
3n 4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 21

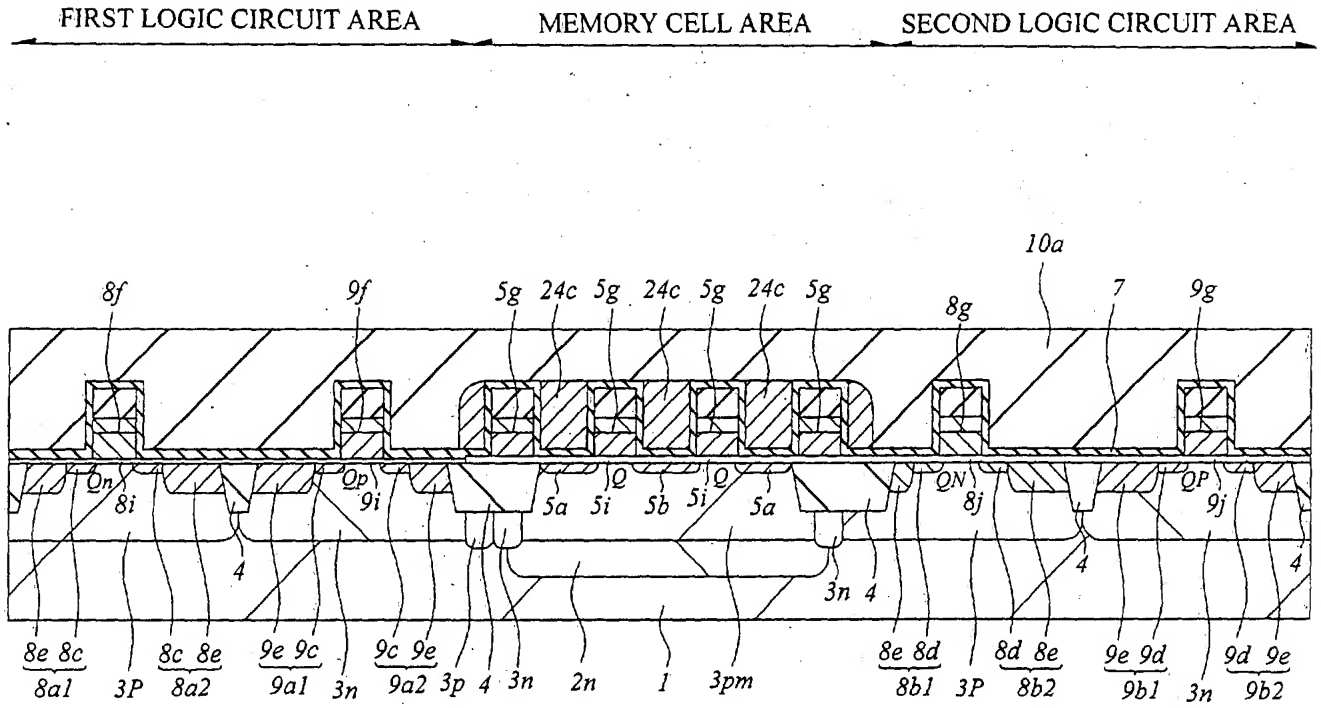
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a
8f
9f
5g 24c 5g 24c 5g 24c 5g
8g
7
9g
Qn
8i
Qp
9i
5a 5i 5b 5i 5a
Q
QN
8j
QP
9j
4
3n 4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 22

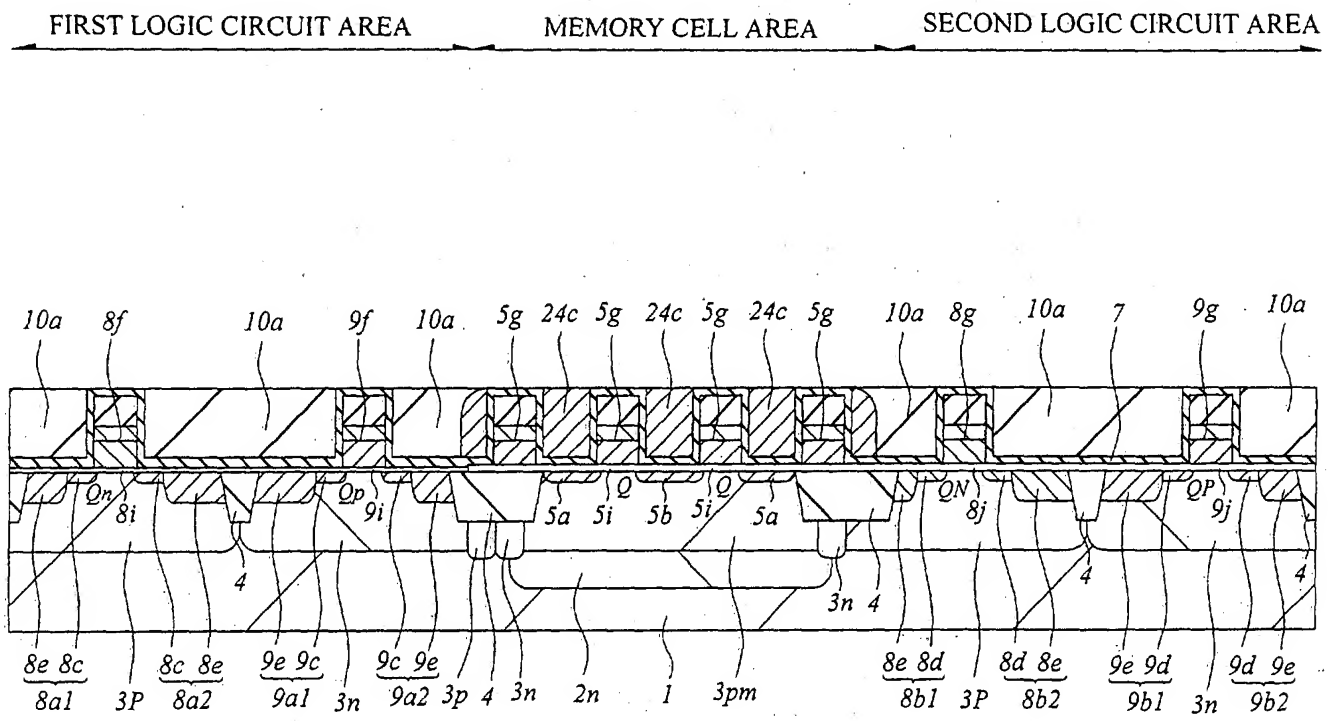
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a 8f 10a 9f 10a 5g 24c 5g 24c 5g 24c 5g 10a 8g 10a 7 9g 10a
Qn 8i Qp 9i Q 5a 5i 5b 5i Q 5a QN 8j QP 9j
4 4 3n 4 4 4
8e 8c 8a1 3P 8c 8e 8a2 9e 9c 9a1 3n 9c 9e 9a2 3p 4 3n 2n 1 3pm 8e 8d 8b1 3P 8d 8e 8b2 9e 9d 9b1 3n 9d 9e 9b2

Fig. 23

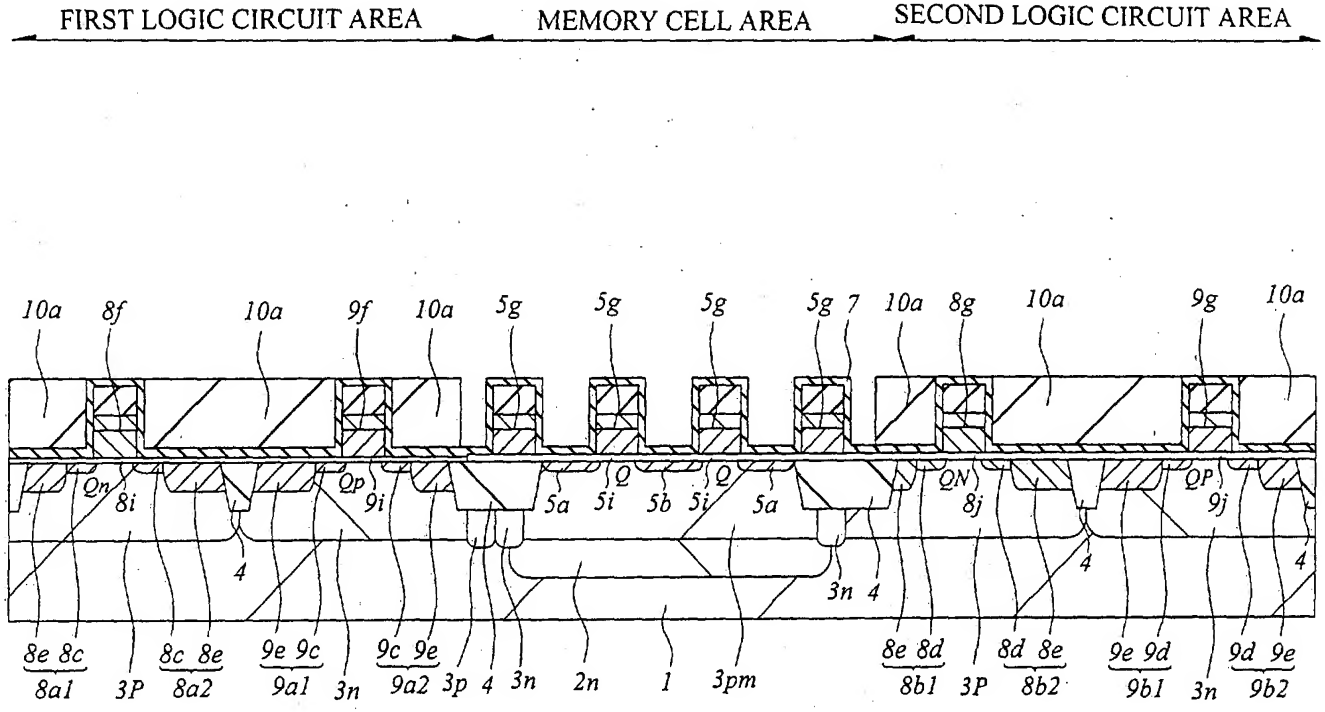
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a 8f 10a 9f 10a 5g 5g 5g 5g 7 10a 8g 10a 9g 10a
Qn 8i Qp 9i 5a 5i Q 5b 5i Q 5a QN 8j QP 9j
4 4 3n 4 4 4
8e 8c / 8a1 3P 8c 8e / 8a2 9e 9c / 9a1 3n 9c 9e / 9a2 3p 4 3n 2n 1 3pm
8e 8d / 8b1 3P 8d 8e / 8b2 9e 9d / 9b1 3n 9d 9e / 9b2

Fig. 24

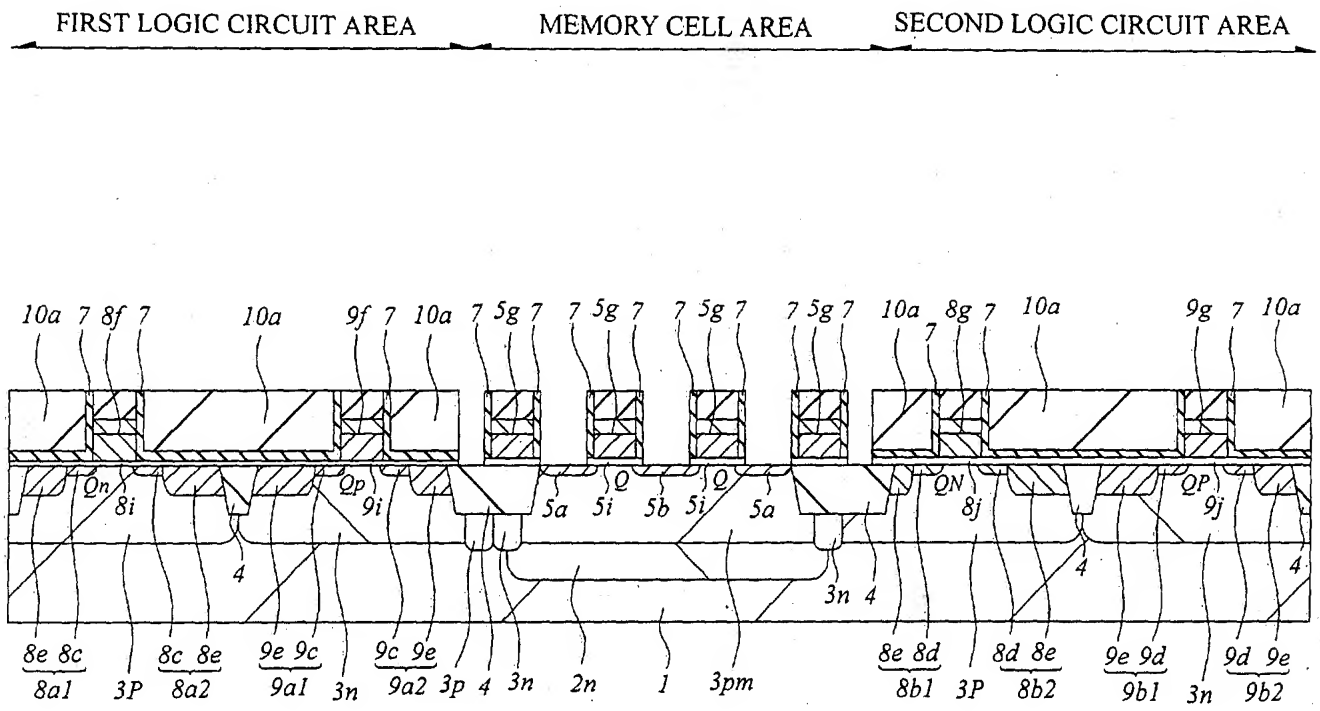
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a 7 8f 7 10a 9f 7 10a 7 5g 7 7 5g 7 7 5g 7 7 5g 7 10a 7 8g 7 10a 9g 7 10a
Qn 8i Qp 9i 5a 5i Q 5b Q 5i 5a QN 8j QP 9j
4 4 3n 4 4 4
8e 8c 8a1 3P 8c 8e 8a2 9e 9c 9a1 3n 9c 9e 9a2 3p 4 3n 2n 1 3pm 8e 8d 8b1 3P 8d 8e 8b2 9e 9d 9b1 3n 9d 9e 9b2

Fig. 25

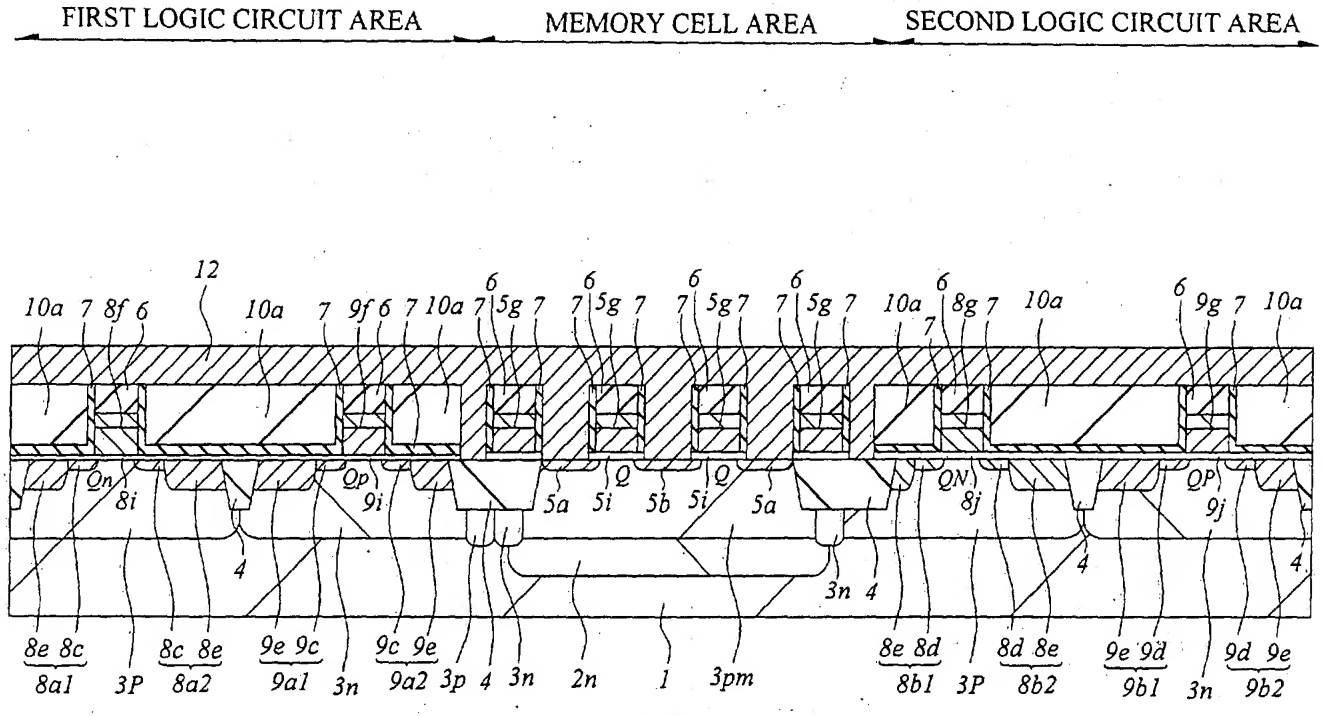
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
12
10a 7 8f 6
10a 7 9f 6 7 10a 7 5g 7 7 5g 7 7 5g 7 7 5g 7 7 5g 7 10a 7 8g 7 10a
6 9g 7 10a
Qn
8i
Qp
9i
5a 5i 5b 5i 5a
Q
Q
QN
8j
QP
9j
4
3n 4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 26

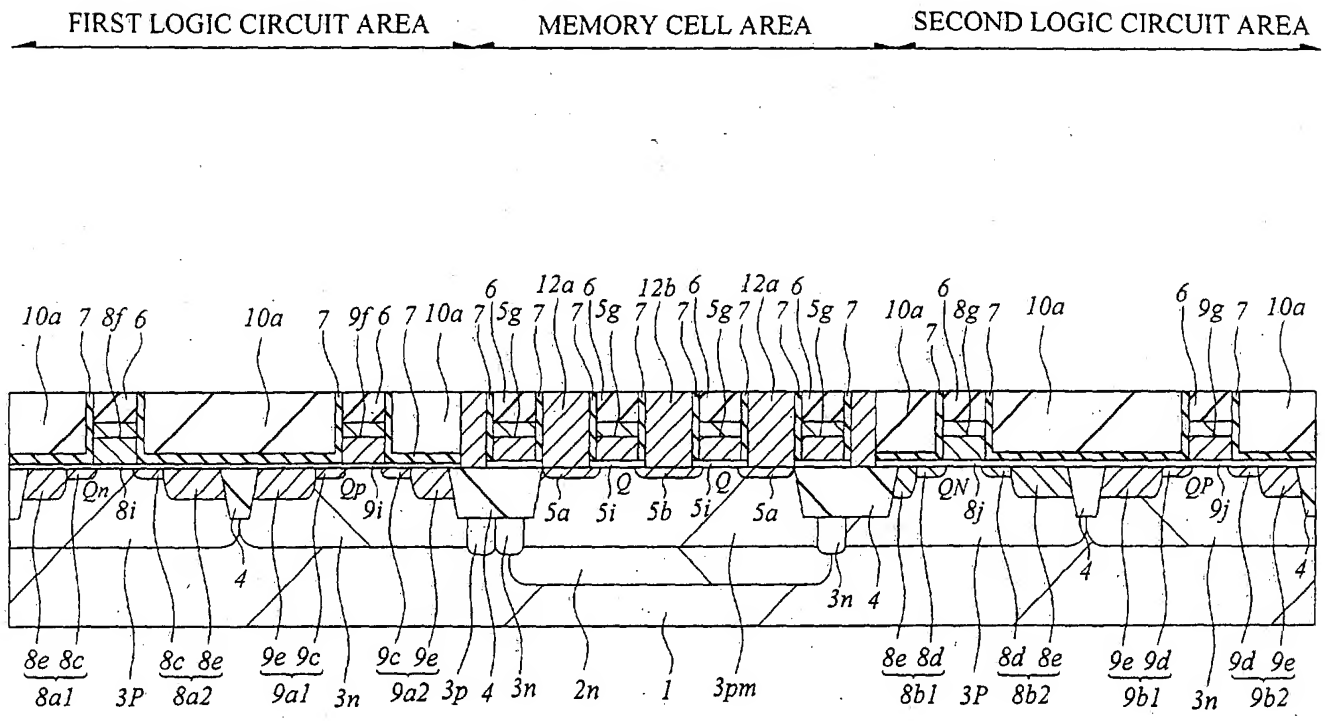
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a 7 8f 6
10a 7 9f 6 7 10a 7 6 5g 7 12a 6 7 5g 7 12b 6 7 5g 7 12a 6 7 5g 7
10a 7 6 8g 7 10a
6 9g 7 10a
Qn 8i
Qp 9i
5a 5i 5b 5i 5a
QN 8j
QP 9j
4
3n 4
8e 8c 8a1
8c 8e 8a2
9e 9c 9a1
9c 9e 9a2
3P 3n 3p 4 3n 2n 1 3pm
8e 8d 8b1
8d 8e 8b2
9e 9d 9b1
9d 9e 9b2
3P 3n

Fig. 27

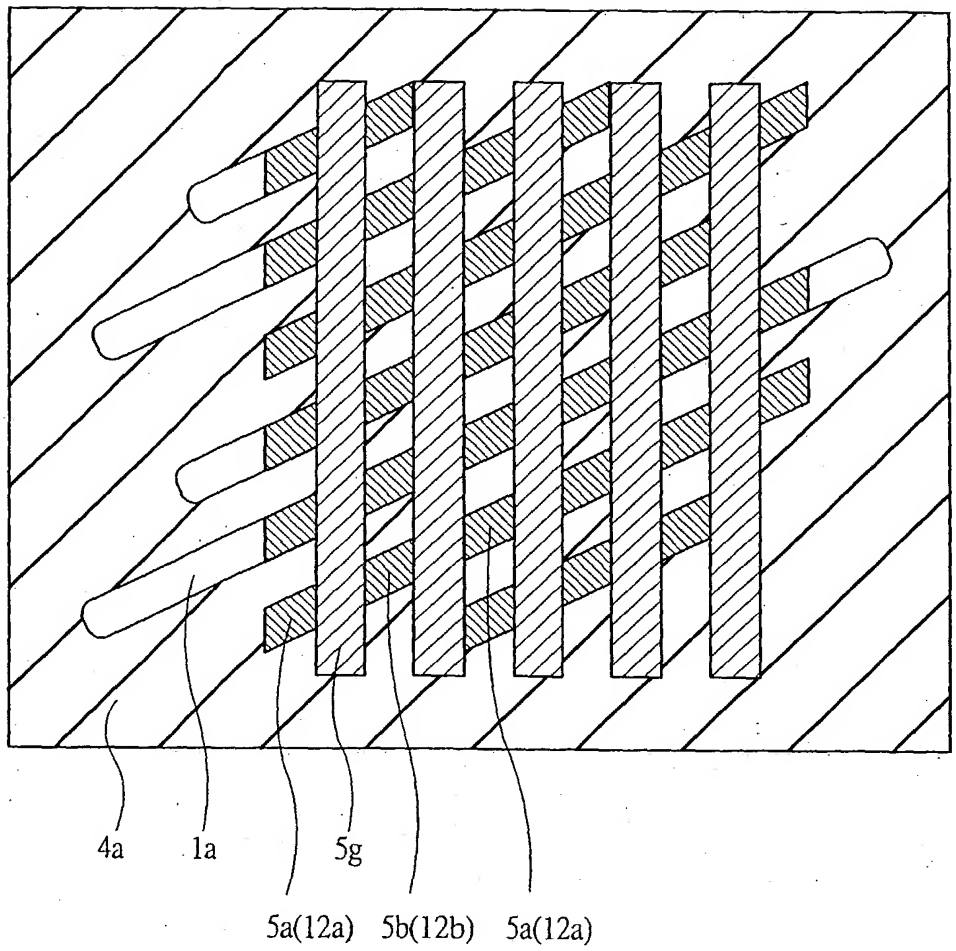

Fig. 28

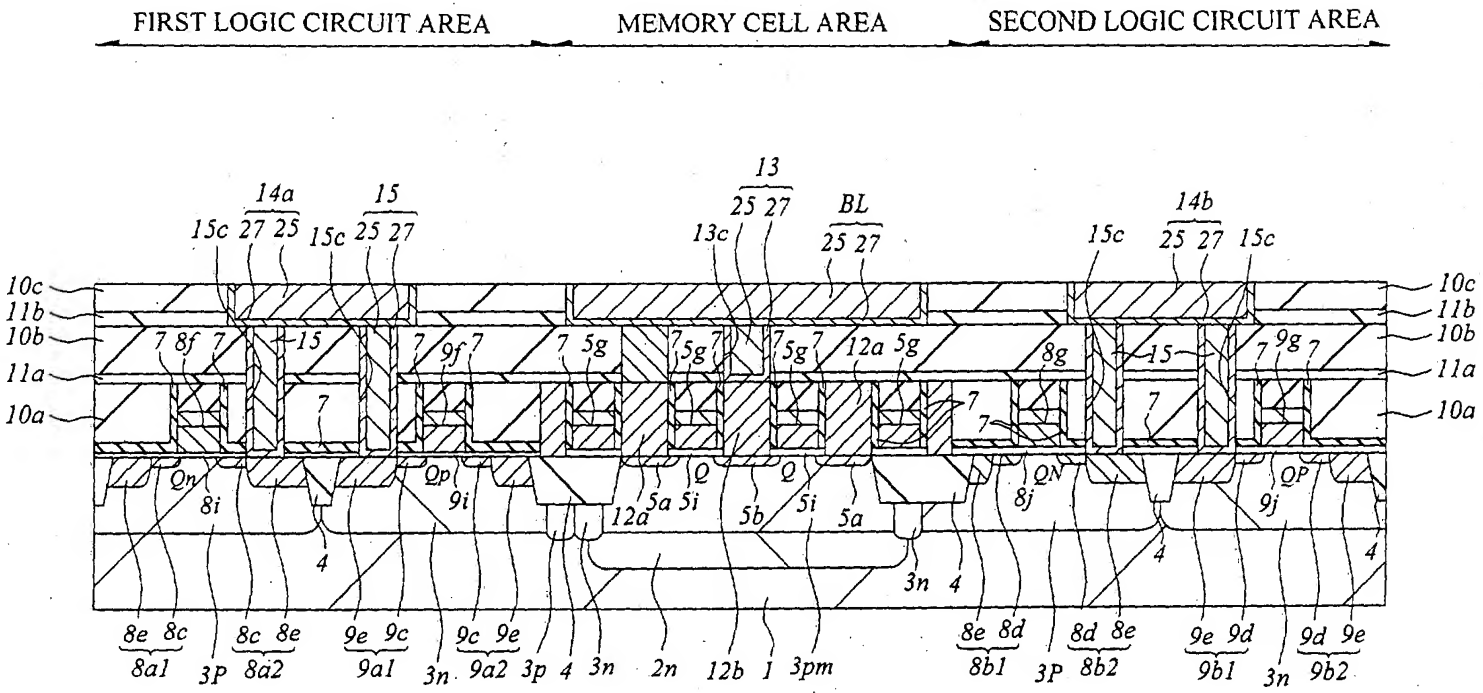
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
14a
15
13
BL
14b
25 27
15c
10c
11b
10b
11a
10a
7
8f
15
9f
5g
12a
8g
9g
Qn
Qp
Q
QN
QP
8i
9i
5a
5i
5b
12a
8j
9j
4
3n
8e 8c
8c 8e
9e 9c
9c 9e
8e 8d
8d 8e
9e 9d
9d 9e
8a1
3P
8a2
9a1
3n
9a2
3p
4
2n
12b
1
3pm
8b1
8b2
9b1
9b2

Fig. 29

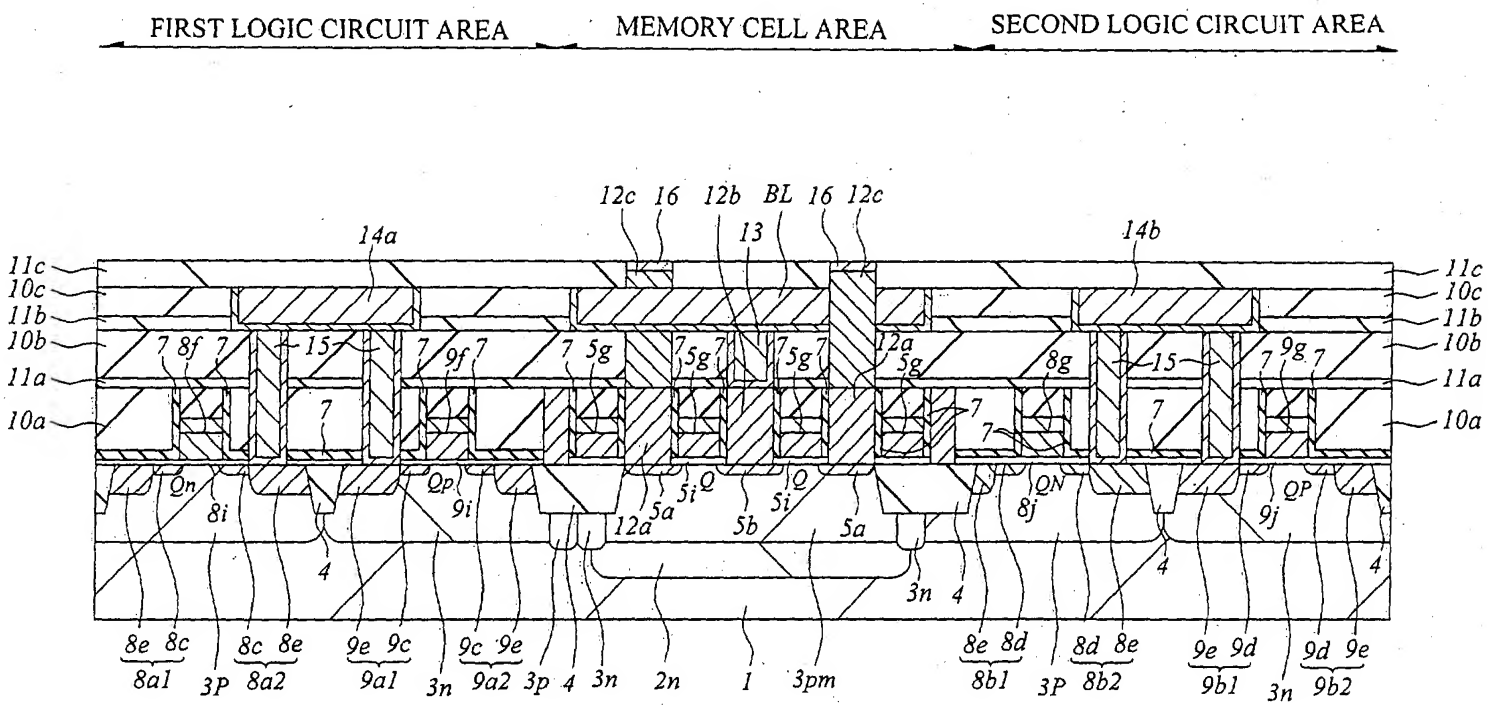
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
12c 16 12b BL 16 12c
14a
13
14b
11c
10c
11b
10b
11a
10a
7 8f 7 15 7 9f 7 7 5g 7 5g 7 5g 7 12a 5g 8g 15 7 9g 7
Qn
8i
Qp
9i
5a 5i Q 5i Q 5b 5a 12a
8j QN 9j QP
4
3n 4
8e 8c 8c 8e 9e 9c 9c 9e 8e 8d 8d 8e 9e 9d 9d 9e
8a1 3P 8a2 9a1 3n 9a2 3p 4 3n 2n 1 3pm 8b1 3P 8b2 9b1 3n 9b2

Fig. 30

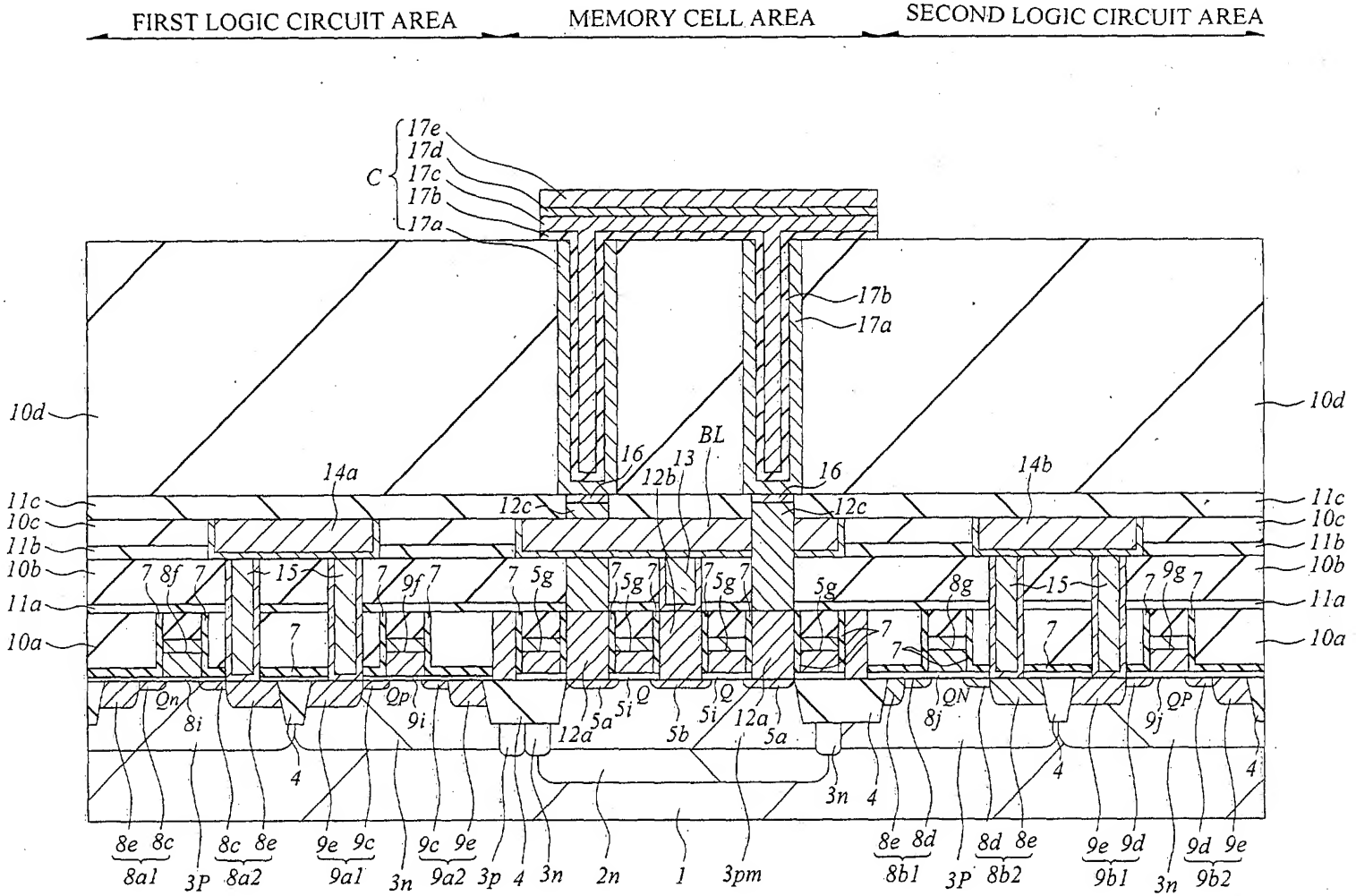
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
C
17e
17d
17c
17b
17a
10d
11c
10c
11b
10b
11a
10a
BL
16
13
12b
14a
14b
12c
15
7
8f
9f
5g
8g
9g
Qn
Qp
QN
QP
8i
9i
8j
9j
5a
5i
Q
5b
12a
4
3n
8e 8c
8c 8e
9e 9c
9c 9e
8e 8d
8d 8e
9e 9d
9d 9e
8a1
3P
8a2
9a1
3n
9a2
3p
2n
1
3pm
8b1
8b2
9b1
9b2

Fig. 31

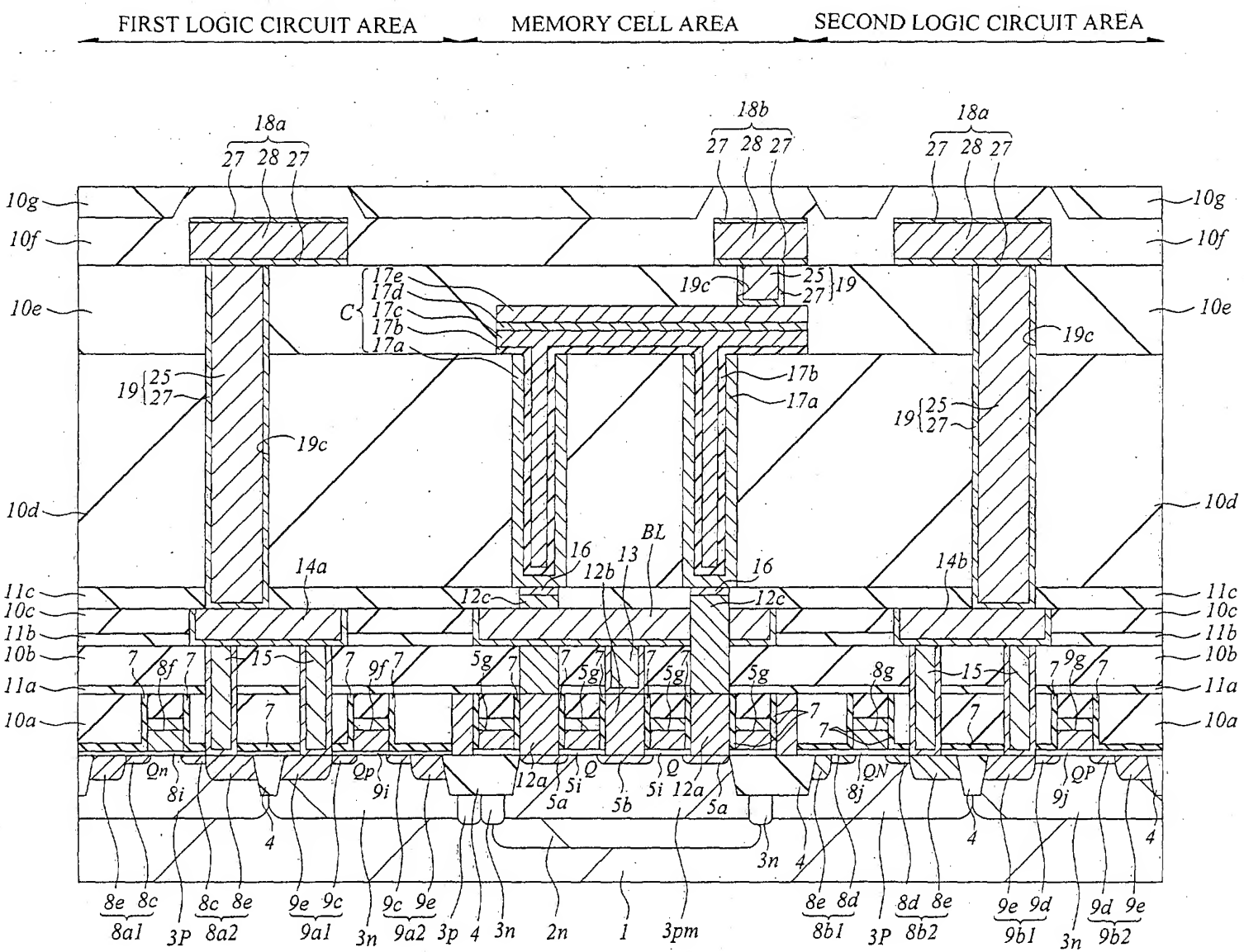
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
18a
18b
27 28 27
10g
10f
10e
10d
10c
11c
11b
10b
11a
10a
17e
17d
17c
17b
17a
C
19
25
27
19c
14a
14b
16
12b
13
BL
12c
12a
5a
5b
5i
5g
15
7
8f
9f
8g
9g
8i
9i
8j
9j
Qn
Qp
QN
QP
Q
4
3n
3p
2n
1
3pm
8e 8c
8a1
8c 8e
8a2
9e 9c
9a1
9c 9e
9a2
8e 8d
8b1
8d 8e
8b2
9e 9d
9b1
9d 9e
9b2

Fig. 32

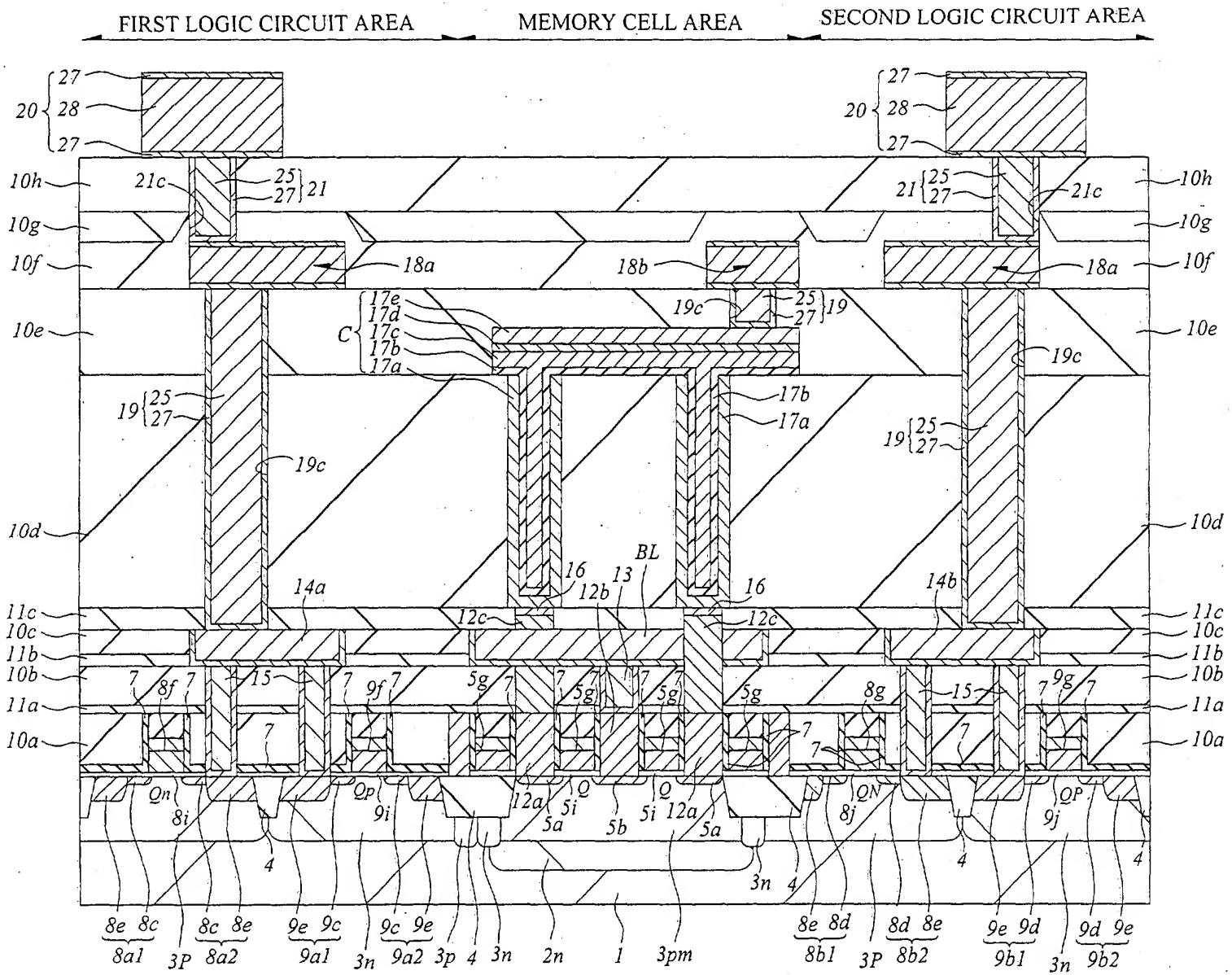
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
20
27
28
27
10h
21c
25
27
21
10g
10f
18a
18b
10e
17e
17d
17c
17b
17a
C
19c
19
BL
16
13
12b
14a
14b
12c
10d
11c
10c
11b
10b
11a
10a
7
8f
15
9f
5g
8g
9g
Qn
8i
Qp
9i
12a
5i
5a
Q
5b
QN
8j
QP
9j
4
3n
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
9c 9e
9a2
3p
2n
1
3pm
8e 8d
8b1
8d 8e
8b2
9e 9d
9b1
9d 9e
9b2

Fig. 33

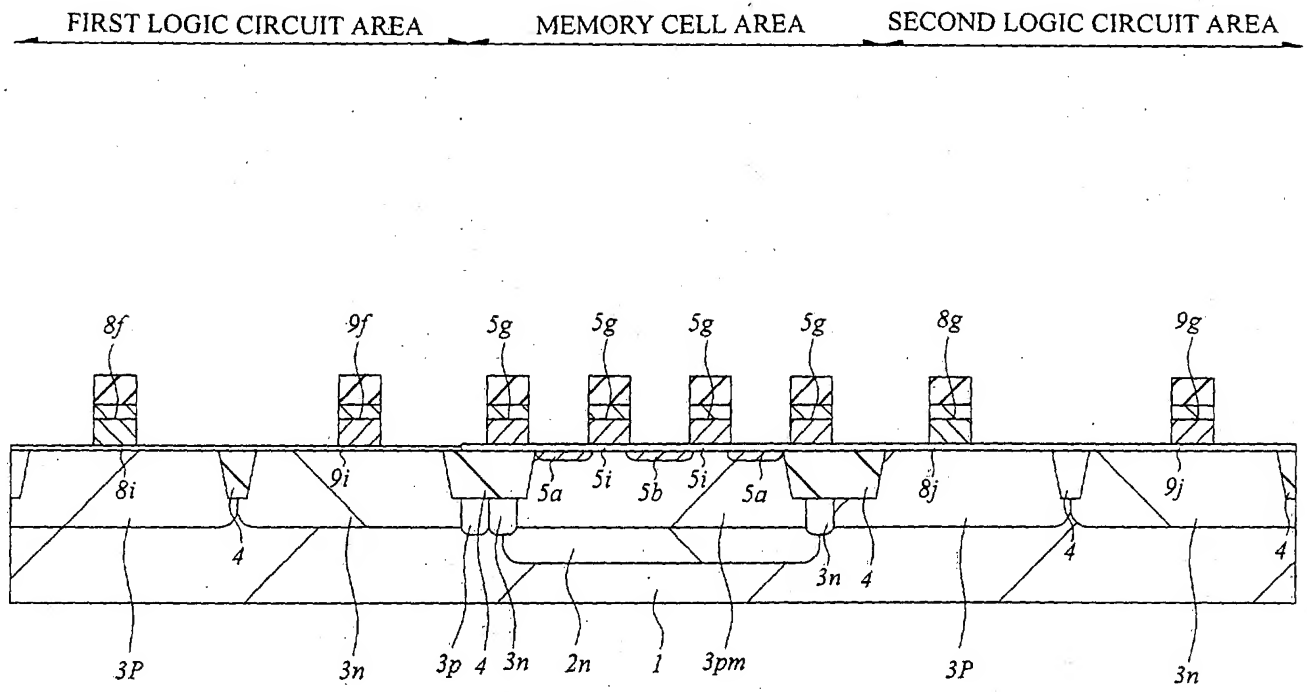
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g
5g
5g
5g
8g
9g
8i
9i
5a
5i
5b
5i
5a
8j
9j
4
4
3n
4
4
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 34

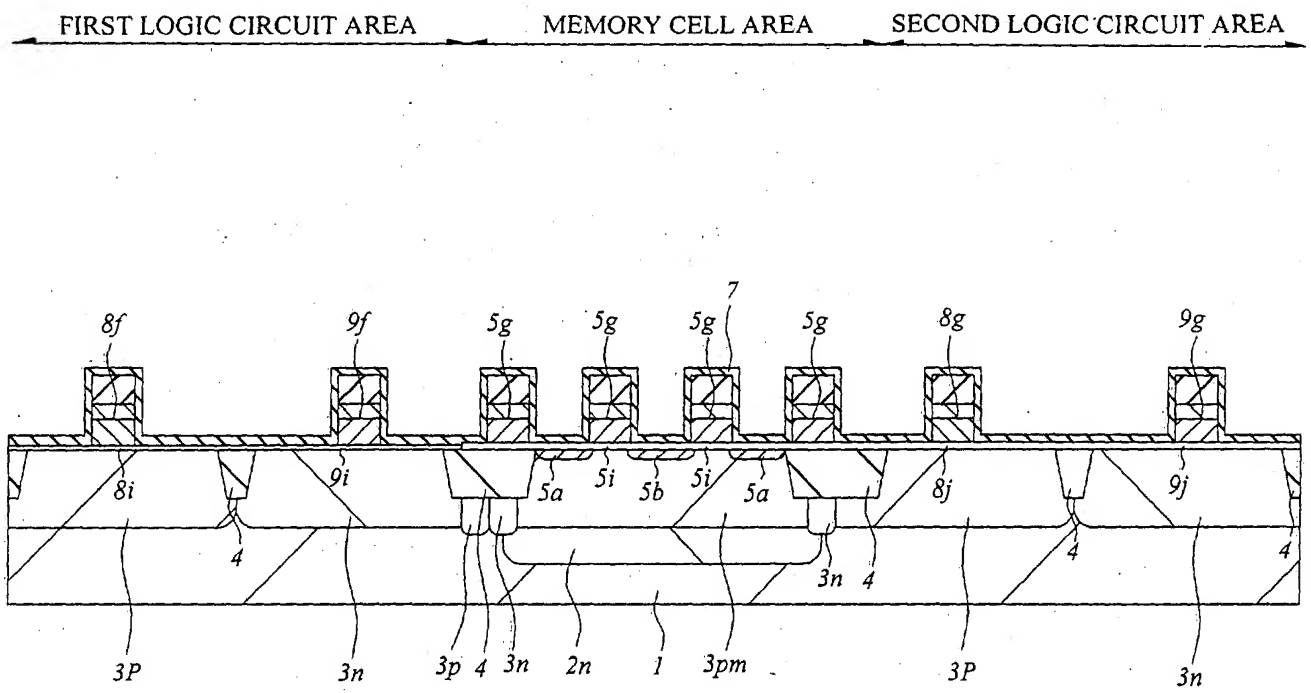
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
7
8f
9f
5g
5g
5g
5g
8g
9g
8i
9i
5a
5i
5b
5i
5a
8j
9j
4
4
3n
4
4
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 35

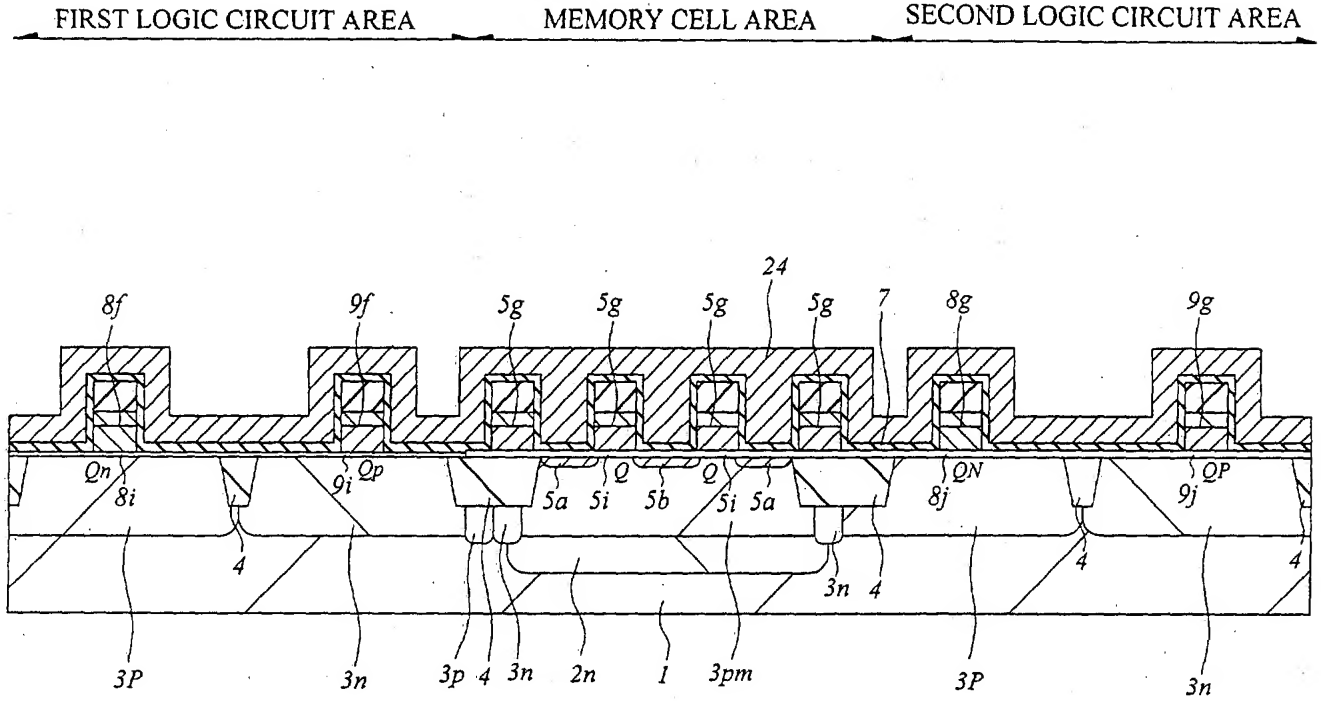
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g
5g
5g
24
5g
7
8g
9g
Qn
8i
9i
Qp
5a
5i
Q
5b
Q
5i
5a
8j
QN
9j
QP
4
4
3n
4
4
4
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 36

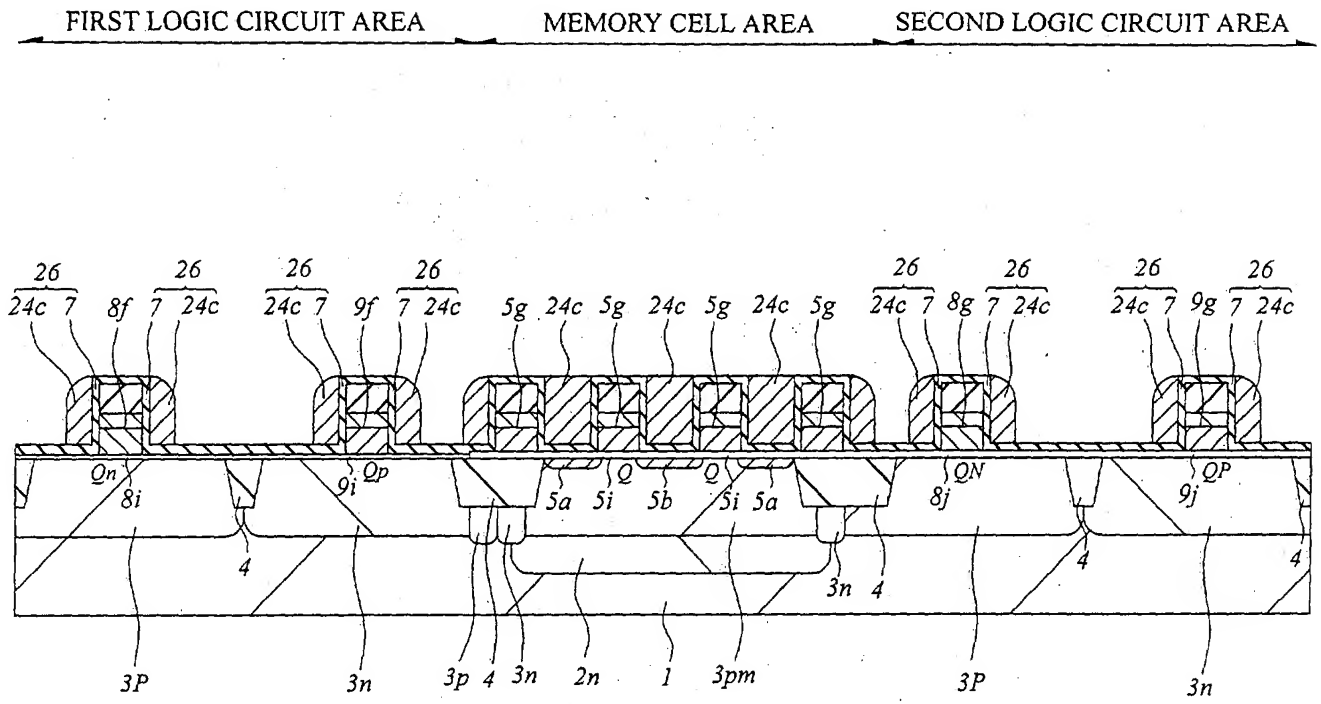
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
26
24c 7
8f
9f
5g 24c 5g 24c 5g 24c 5g
8g
9g
Qn
Qp
Q
QN
QP
8i
9i
5a 5i 5b 5i 5a
8j
9j
4
3n 4
3P
3n
3p 4 3n
2n
1
3pm

Fig. 37

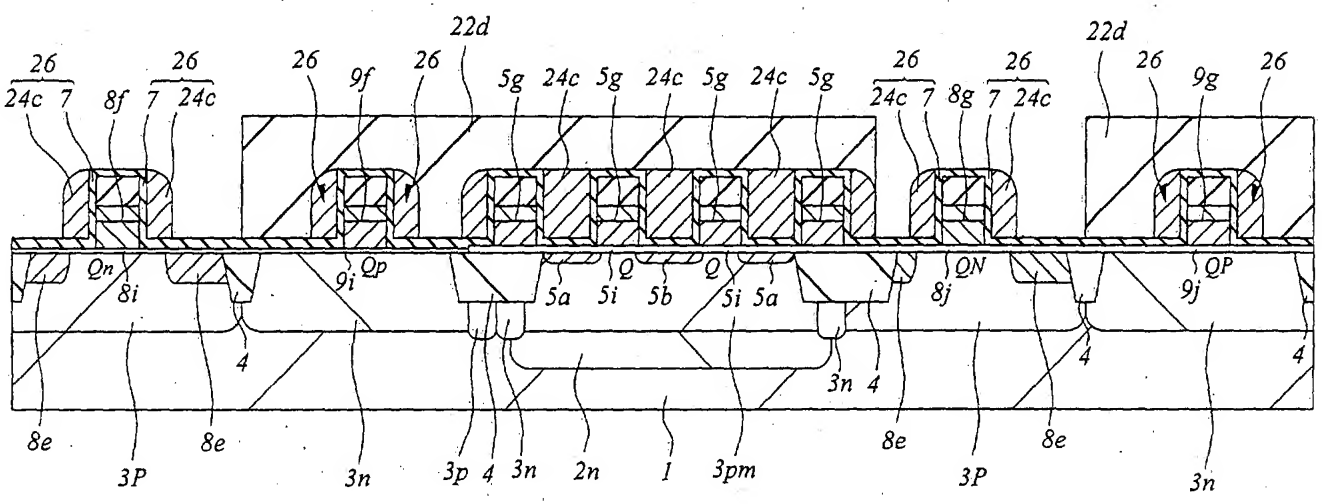
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
26
24c
7
8f
22d
9f
5g
24c
8g
9g
Qn
8i
Qp
9i
Q
5a
5i
5b
QN
8j
QP
9j
4
8e
3P
3n
3p
2n
1
3pm

Fig. 38

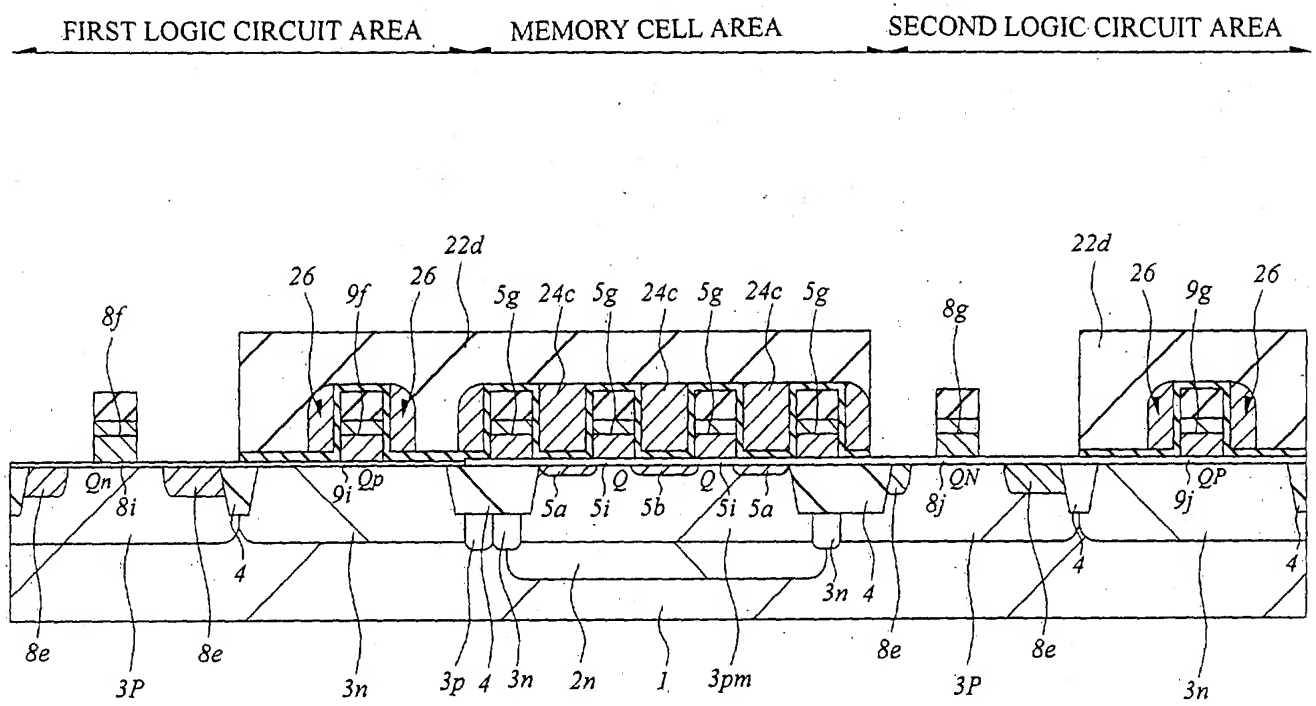
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22d
26
9f
26
22d
26
9g
26
5g
24c
5g
24c
5g
24c
5g
8f
8g
Qn
8i
9i
Qp
5a
5i
Q
5b
Q
5i
5a
8j
QN
9j
QP
4
4
4
3n
4
8e
8e
8e
8e
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 39

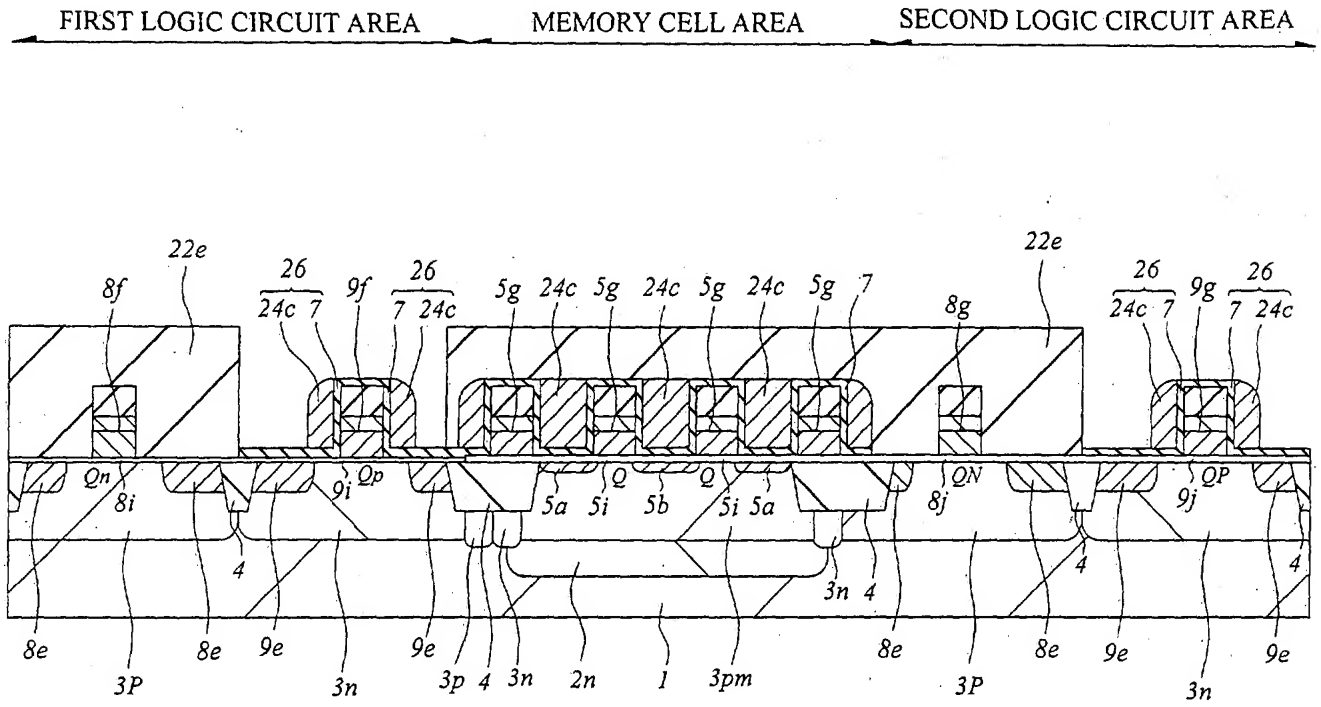
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22e
8f
26
24c 7
9f
26
7 24c
5g 24c 5g 24c 5g 24c 5g 7
8g
22e
26
24c 7
9g
26
7 24c
Qn
8i
9i
Qp
5a 5i 5b 5i 5a
Q
Q
8j
QN
9j
QP
4
3n 4
8e
3P
8e
9e
3n
9e
3p 4 3n
2n
1
3pm
8e
3P
8e
9e
3n
9e

Fig. 40

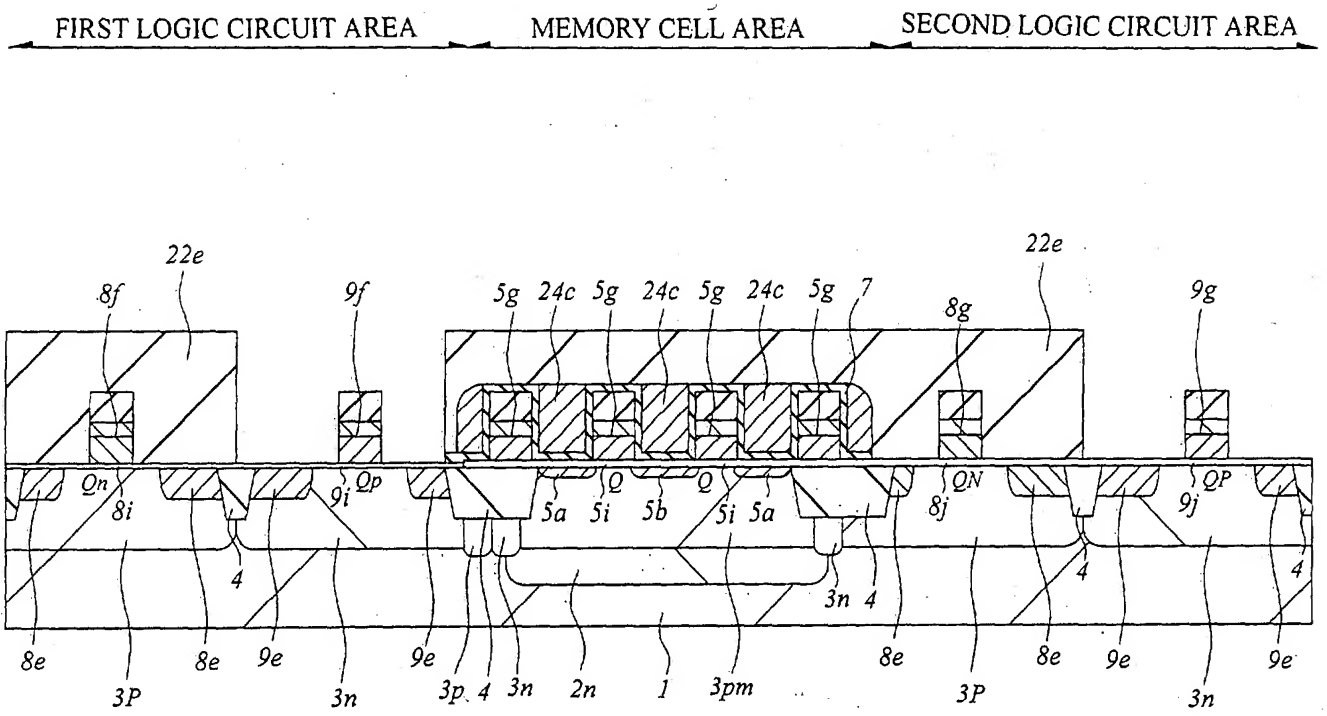
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22e
8f
9f
5g 24c 5g 24c 5g 24c 5g 7
8g
22e
9g
Qn
8i
9i
Qp
5a 5i 5b
Q
5i 5a
8j
QN
9j
QP
4
3n 4
4
4
8e
3P
8e
9e
3n
9e
3p 4 3n
2n
1
3pm
8e
3P
8e
9e
3n
9e

Fig. 41

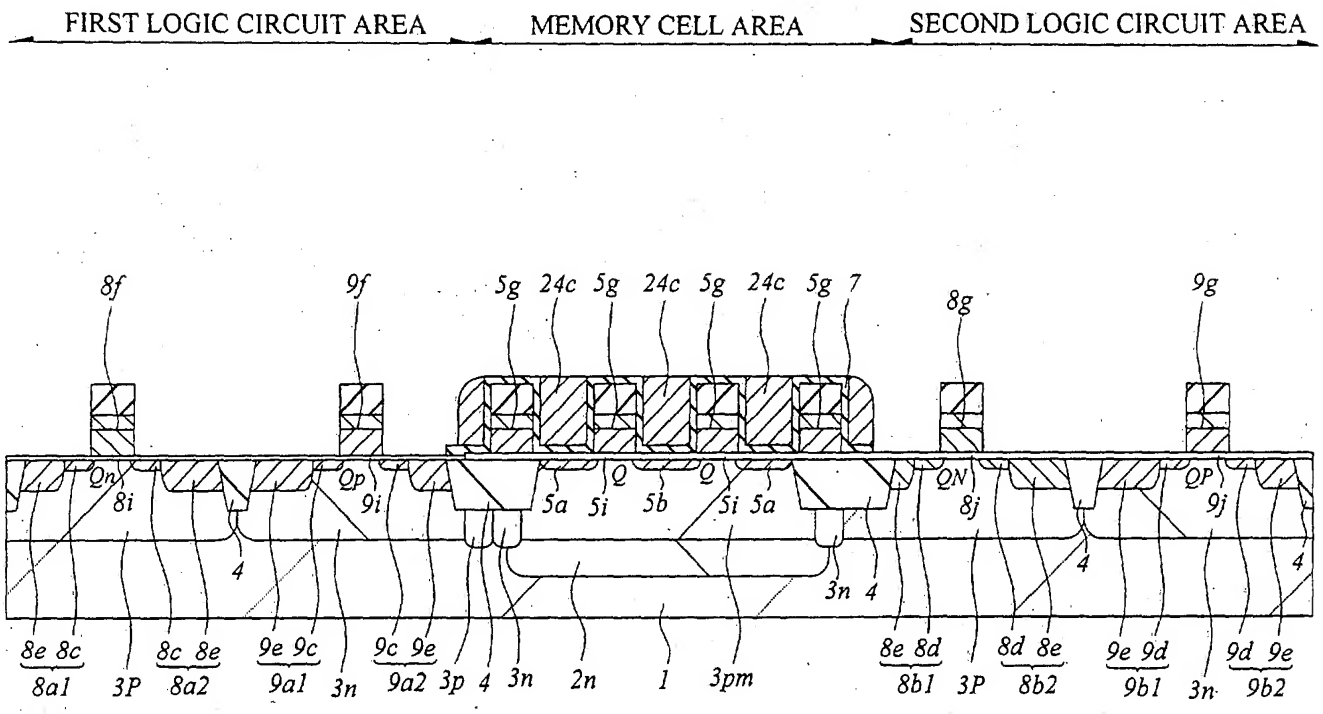
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
8f
9f
5g 24c 5g 24c 5g 24c 5g 7
8g
9g
Qn
8i
Qp
9i
5a 5i 5b 5i 5a
QN
8j
QP
9j
4
3n 4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 42

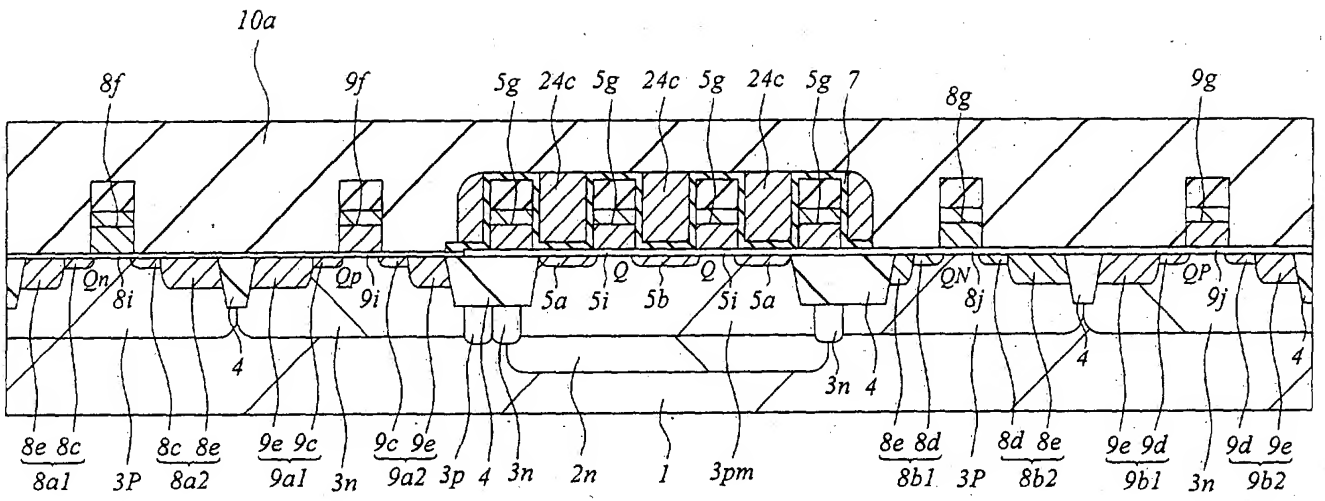
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a
8f
9f
5g 24c 5g 24c 5g 24c 5g 7
8g
9g
Qn
8i
Qp
9i
5a 5i 5b
Q
Q
5i 5a
QN
8j
QP
9j
4
4
3n 4
4
4
8e 8c
8a1
3P
8c 8e
8a2
9e 9c
9a1
3n
9c 9e
9a2
3p 4 3n
2n
1
3pm
8e 8d
8b1
3P
8d 8e
8b2
9e 9d
9b1
3n
9d 9e
9b2

Fig. 43

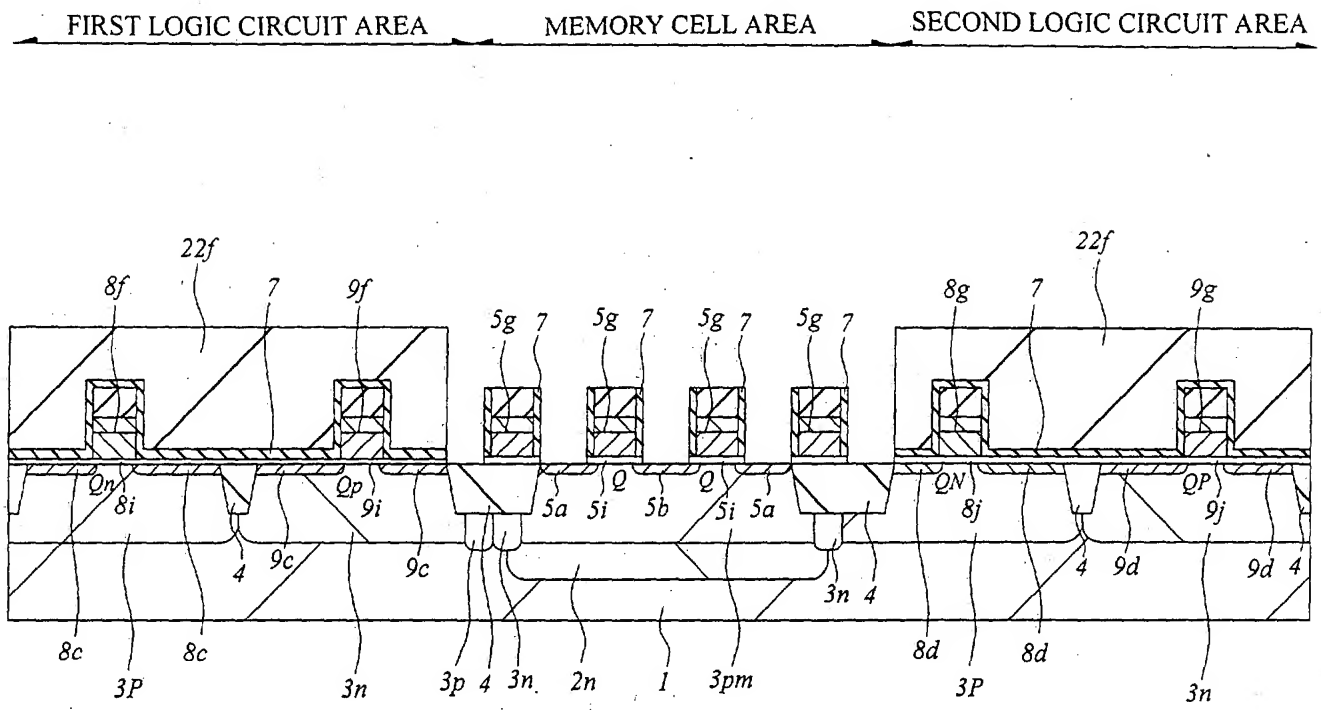
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22f
8f
7
9f
5g 7
5g 7
5g 7
5g 7
8g
7
22f
9g
Qn
8i
Qp
9i
5a 5i 5b
Q
Q
5i 5a
QN
8j
QP
9j
4
9c
9c
3n 4
4 9d
9d 4
8c
3P
8c
3n
3p 4 3n
2n
1
3pm
8d
3P
8d
3n

Fig. 44

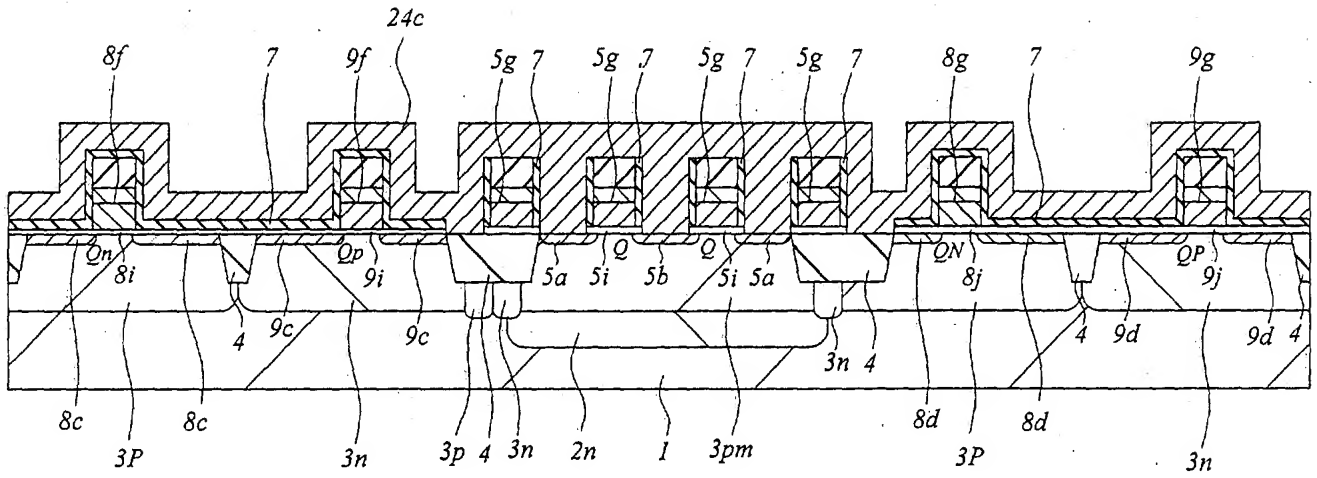
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
24c
8f
7
9f
5g
7
5g
7
5g
7
5g
7
8g
7
9g
Qn
8i
Qp
9i
5a
5i
Q
5b
Q
5i
5a
QN
8j
QP
9j
4
9c
9c
3n
4
4
9d
9d
4
8c
8c
3P
3n
3p
4
3n
2n
1
3pm
8d
8d
3P
3n

Fig. 45

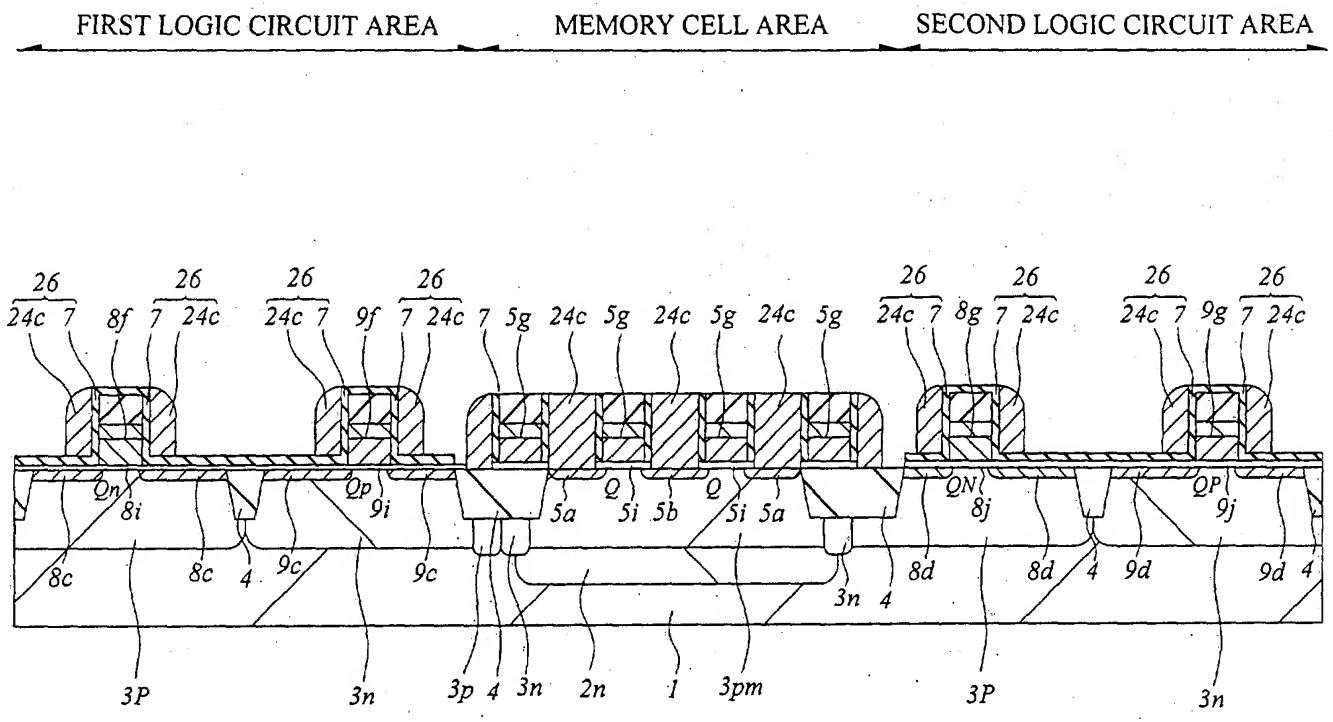
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
26
24c 7 8f 7 24c
24c 7 9f 7 24c
7 5g 24c 5g 24c 5g 24c 5g
24c 7 8g 7 24c
24c 7 9g 7 24c
Qn
8i
Qp
9i
Q
5a 5i 5b 5i 5a
QN
8j
QP
9j
8c
4
9c
3n
4
8d
4
9d
3P
3n
3p
4
3n
2n
1
3pm
3P
3n

Fig. 46

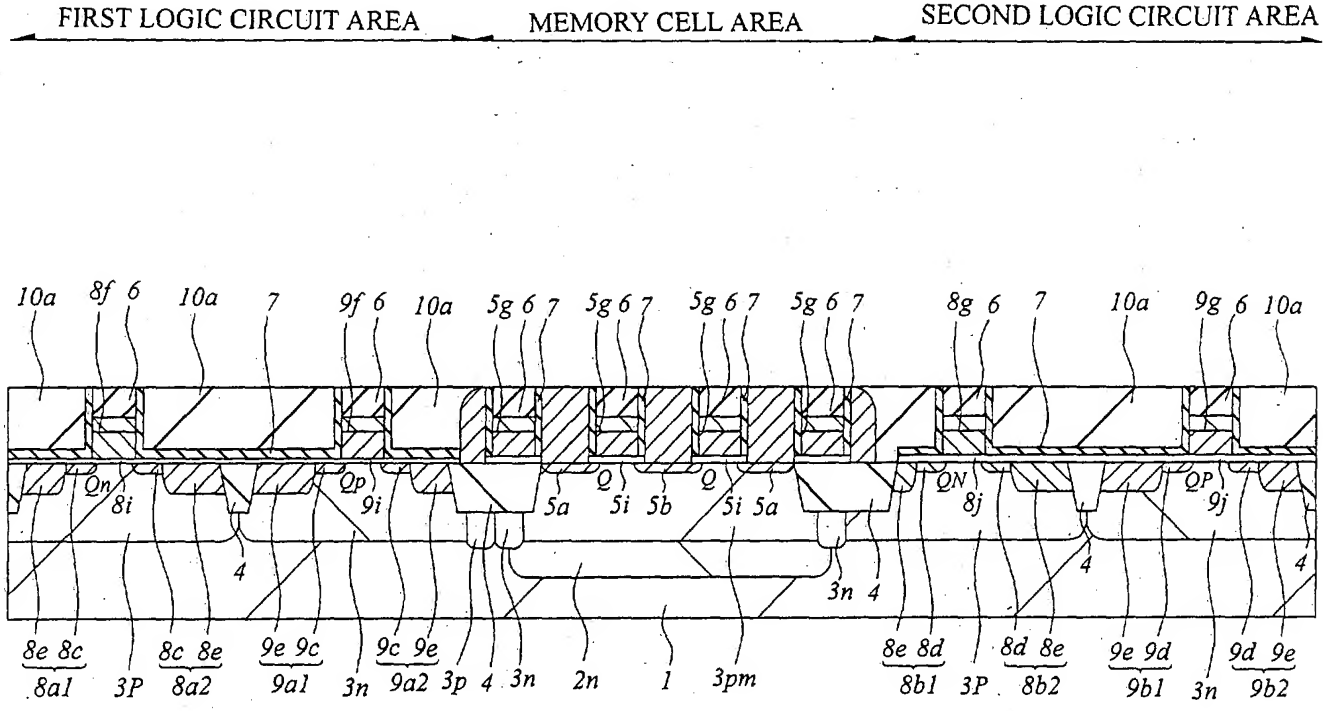
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
10a 8f 6 10a 7 9f 6 10a 5g 6 7 5g 6 7 5g 6 7 5g 6 7 8g 6 7 10a 9g 6 10a
Qn 8i Qp 9i 5a Q 5i 5b Q 5i 5a QN 8j QP 9j
4 4 3n 4 4
8e 8c 8a1 3P 8c 8e 8a2 9e 9c 9a1 3n 9c 9e 9a2 3p 4 3n 2n 1 3pm 8e 8d 8b1 3P 8d 8e 8b2 9e 9d 9b1 3n 9d 9e 9b2

Fig. 47

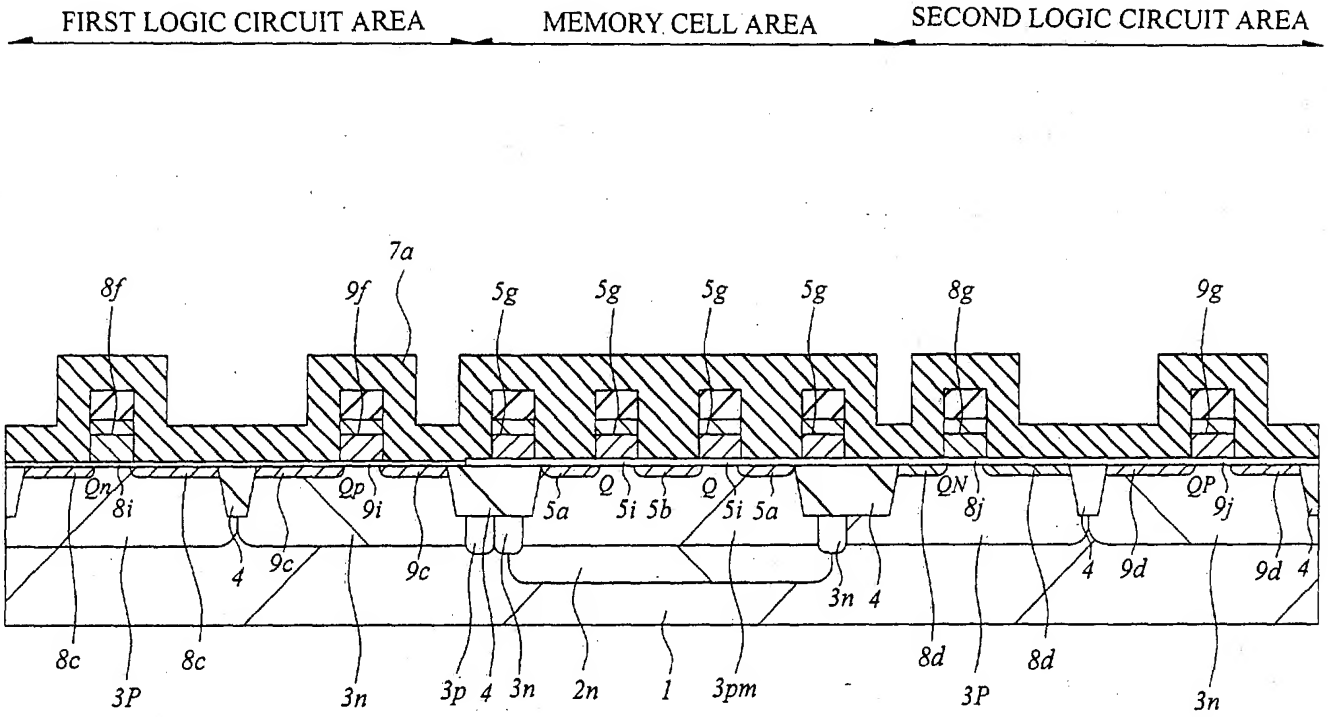
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
7a
8f
9f
5g
5g
5g
5g
8g
9g
Qn
8i
Qp
9i
5a
Q
5i
5b
Q
5i
5a
QN
8j
QP
9j
4
9c
9c
4
9d
9d
4
3n
4
8c
8c
3P
3n
3p
4
3n
2n
1
3pm
8d
8d
3P
3n

Fig. 48

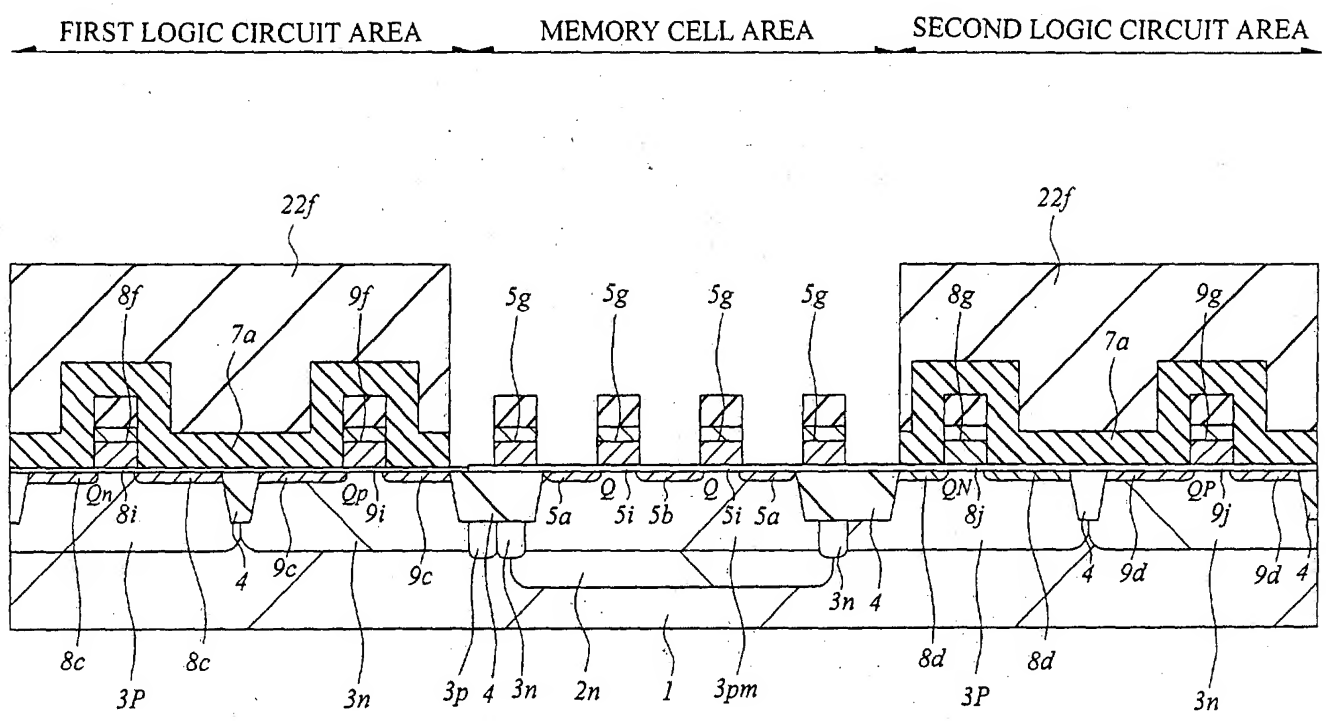
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
22f
22f
8f
9f
7a
5g
5g
5g
5g
8g
9g
7a
Qn
8i
Qp
9i
Q
5a
5i
5b
Q
5i
5a
QN
8j
QP
9j
4
9c
9c
4
3n
4
4
9d
9d
4
8c
3P
8c
3n
3p
4
3n
2n
1
3pm
8d
3P
8d
3n

Fig. 49

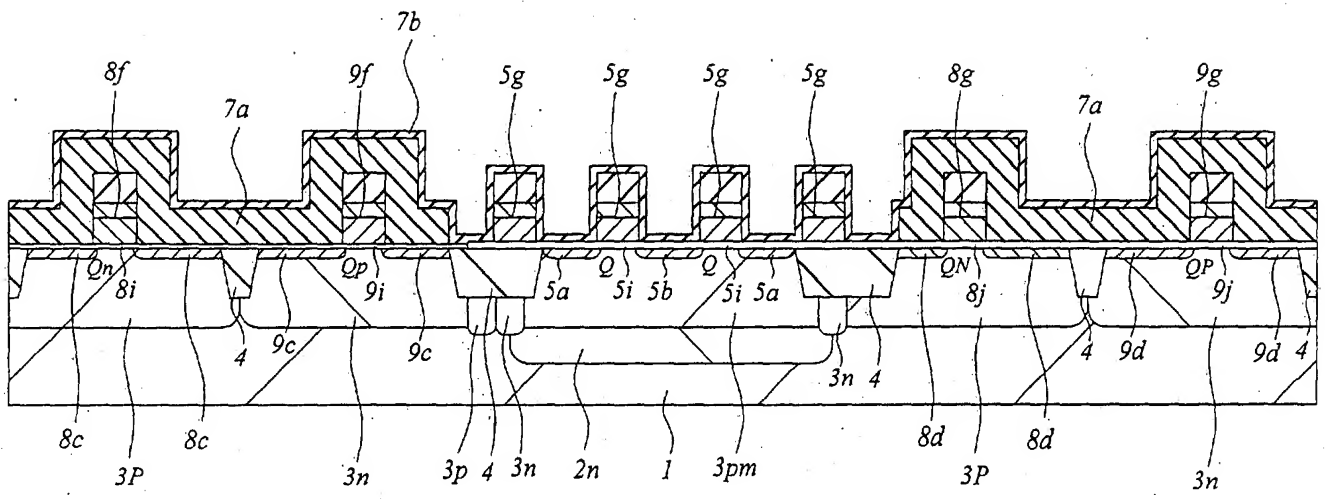
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
7b
8f
9f
5g
5g
5g
5g
8g
9g
7a
7a
Qn
8i
Qp
9i
Q
5i
5b
Q
5i
5a
QN
8j
QP
9j
5a
4
9c
9c
4
9d
9d
4
3n
4
8c
8c
3P
3n
3p
4
3n
2n
1
3pm
8d
8d
3P
3n

Fig. 50

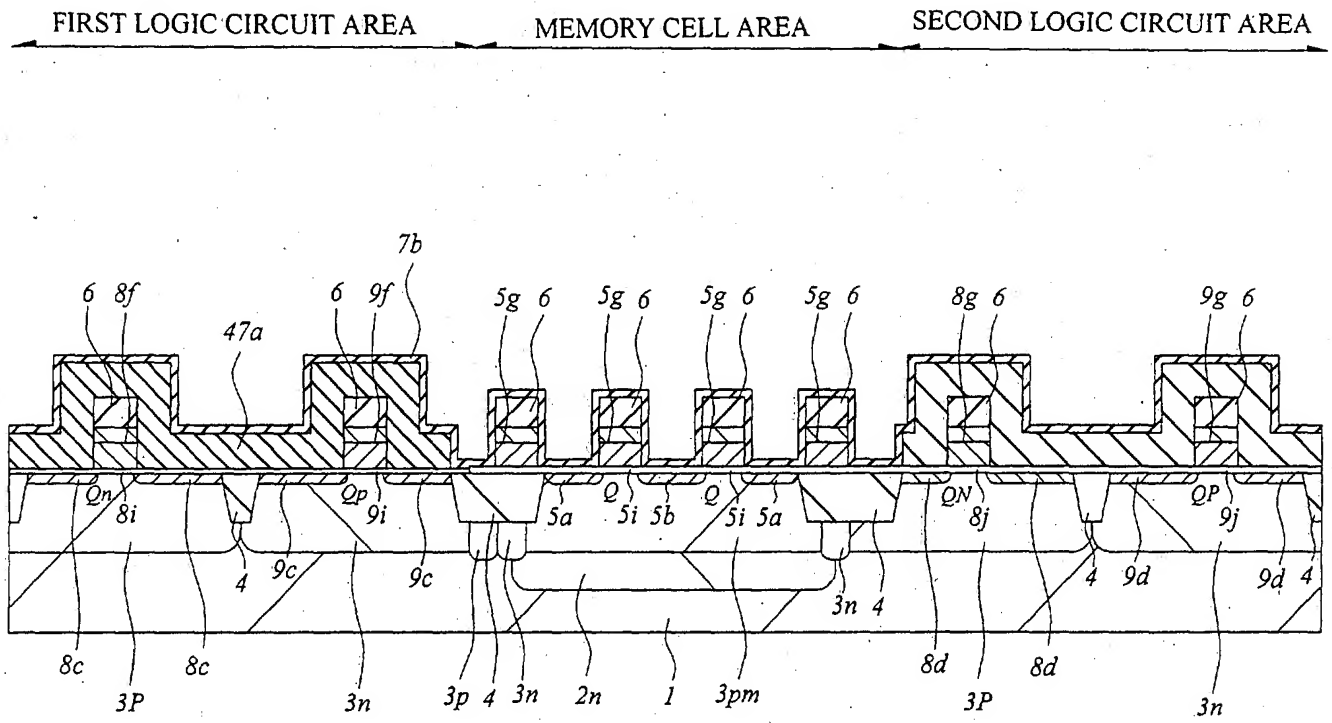
FIRST LOGIC CIRCUIT AREA
MEMORY CELL AREA
SECOND LOGIC CIRCUIT AREA
7b
6 8f
47a
6 9f
5g 6
5g 6
5g 6
5g 6
8g 6
9g 6
Qn
8i
Qp
9i
5a
Q
5i 5b
Q
5i 5a
QN
8j
QP
9j
4
9c
9c
3n 4
4
9d
9d 4
8c
8c
3P
3n
3p 4 3n
2n
1
3pm
8d
8d
3P
3n

Fig. 51

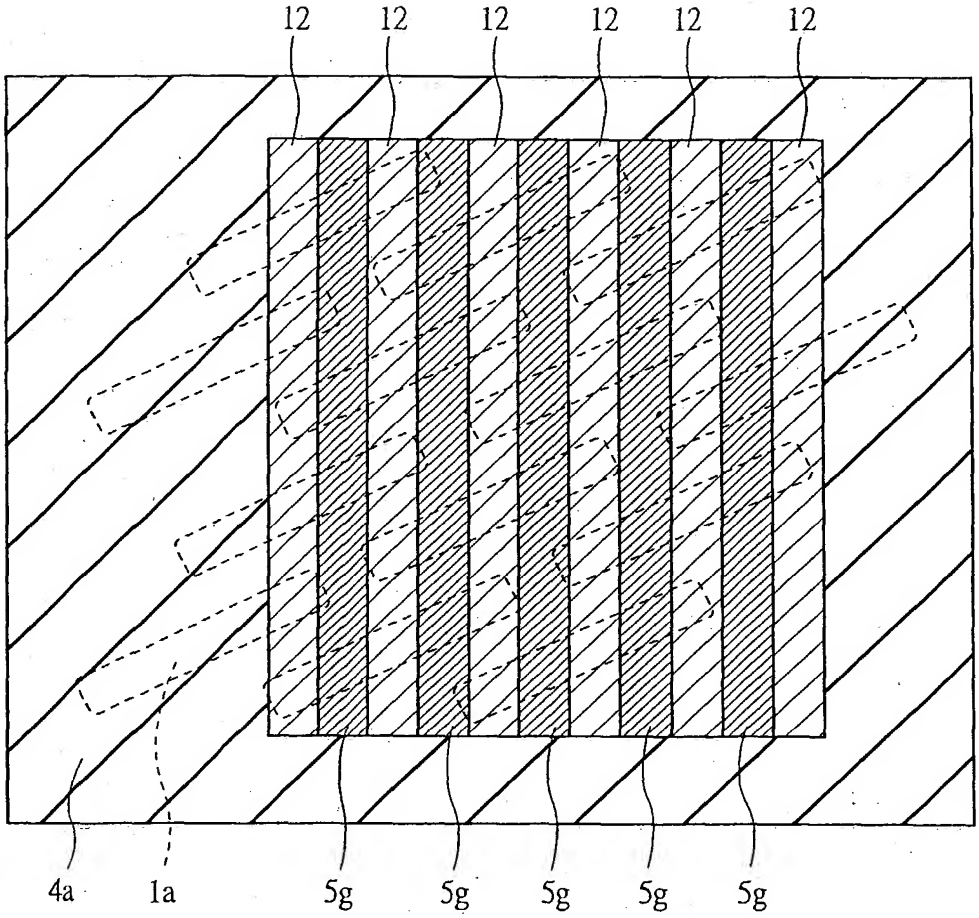

Fig. 52